ENERGY MANAGEMENT SYSTEM

By

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Report for the Course ECE547

(in Electrical and Computer Engineering)

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An Abstract of the Report Presented
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The Energy Management System (EMS) are used in variety of applications ranging from RFID to Wireless Sensor Networks (WSN). The EMS provides the power supply to the functional design in devices without batteries. The Energy Harvesting Circuit (EHC) generates varying charge (current) that acts as input to the EMS. This current varies from few nano amperes to microamperes. The current is converted to a constant supply voltage for functional design. The ItoV Converters, comparators, external resistors and external capacitors are used to realize EMS. The design is implemented in cadence 180nm technology with IBM libraries. Also, Electro Static Discharge (ESD) diodes are used for protection. Four designs are implemented in the chip of area 1.5mm X 1.5mm. The DRC, LVS, floating gates and pattern density checks are performed on the chip. The simulations results are executed on the chip after RLCK extraction. The supply voltage is constant for about 4 sec with a load 800Ω.

ACKNOWLEDGMENTS

I would like to express my appreciation and gratitude to those, without whom the project would not be possible.

I am highly indebted to Professor David E. Kotecki for his supervision and encouragement as well as for providing necessary orientation regarding the project and also for support in executing the project.

I am also extremely thankful to Professor Nuri Emanetoglu suggestions regarding the project.

I also acknowledge with admiration, my gratitude towards my parents and family members who always have supported me.

I will be thankful to all my friends who supported me directly or indirectly in completion of this project.

Finally, I would be grateful to professor Venkata Ramani, Mohan Sundaram and Ramasaami for encouraging me to continue my career in microelectronics.

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Circuit Implementation

1.1 Introduction

The Energy Management Systems (EMS) play an important role in generating the supply voltage to the circuits. They are used in wide applications ranging from Radio Frequency IDentification (RFID) to Wireless Sensor Networks (WSN). The work in this report implements EMS in cadence 180nm technology with Electro Static Discharge (ESD) diodes for protection. This chapter gives the details and simulation results of individual circuits used in the project. The chapter is organized as follows :

1. Energy Management Circuit Implementation
2. ItoV Converter
3. Comparator
4. Switching Circuit

The EMS circuit is placed between the Energy Harvesting Circuit (EHC) [1] and the functional design [2], and the block diagram is shown in figure 1.1. The EHC has an input of 150mV at a frequency of 75MHz and produces an output of 1.75V across a load capacitance of 1pF with a charging time of 75ns. Therefore, the output voltage of EHC is converted into varying charge (this develops current). If the load capacitance increases, the time to reach the output voltage to 1.75V increases. The developed charge by the capacitor is given as input to the EMS. The EMS generates the supply voltage to the functional design (Morse code ROM and transmitter).

Two EMS designs are implemented in this work with two ItoV Converter configurations :

1. ItoV Converter with three diodes
2. ItoV Converter with four diodes

Figure 1.1. Placement of EMS between EHC and functional design.

1.2 Energy Management System Implementation

The input current to the EMS is given by EHC. This current varies from few nano amperes to micro amperes. The block diagram of EMS is shown in figure 1.2.

There are two ItoV Converters :

1. First EHC gives the supply voltage to comparator
2. Second EHC gives the control voltage (one of the input) to the comparator and also gives the required supply to the functional design.

The section 1.3, sectin 1.4, section 1.5 describes the blocks in EMS.

1.3 ItoV Converter

The ItoV Converter takes the input charge from EHC and converts the charge to the voltage by using diodes and capacitor. The diodes used in this design are varactor diodes present in cadence 180nm technology. The diodes have widths and lengths of 1μm and 15 anode fingers.

1.3.1 ItoV Converter with three diodes

The three diode configuration generates the voltage of about 1.9V. As mentioned, two ItoV Converter with 100μF and 100mF capacitors across them. The time taken to charge 100mF is higher than 100μF. The schematic and layout diagram of three diode configuration is shown in figure 1.3 and figure 1.4.

The simulation results for three diode ItoV converter configuration for input currents 100nA and 1mA are also presented in this section. First, simulation results for 100nA current are shown in figure 1.5 and 1.6. Secondly, simulation results for 1mA current are shown in figure 1.7 nd 1.8. For 100nA of input current, the charging time for the 100μF capacitor to reach 1.9V is 2.0Ks and the charging time for 100mF capacitor

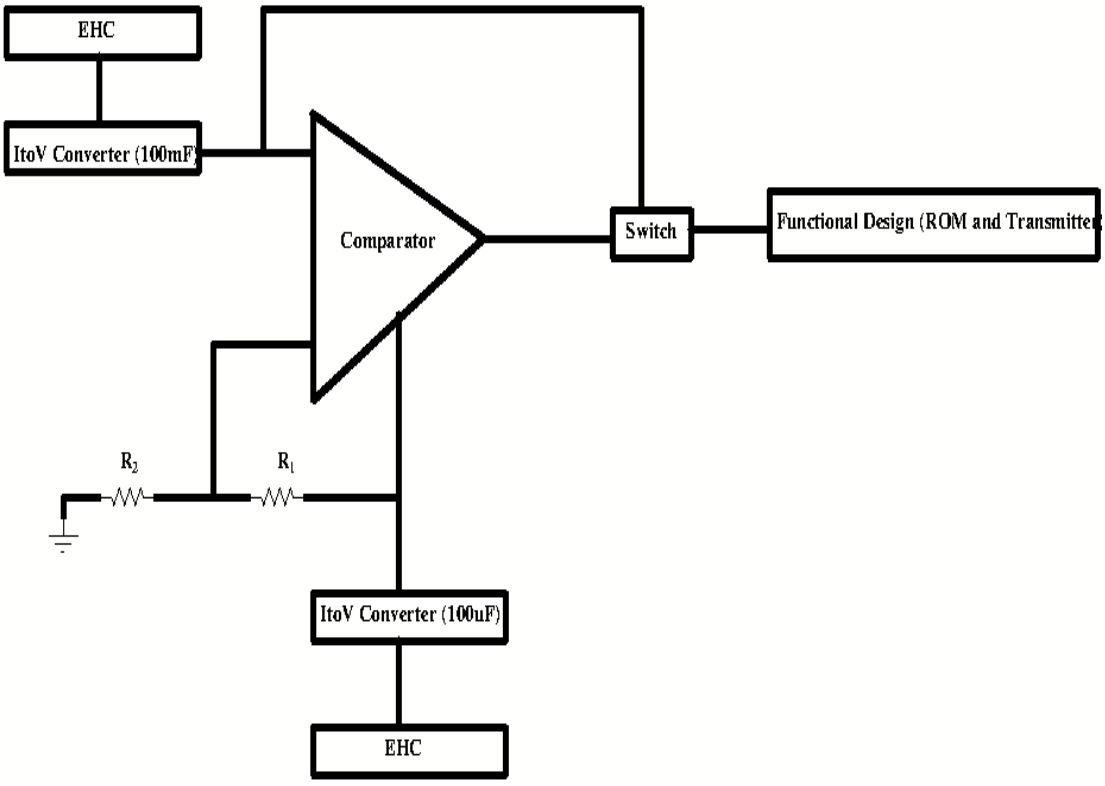

Figure 1.2. Block diagram of EMS.

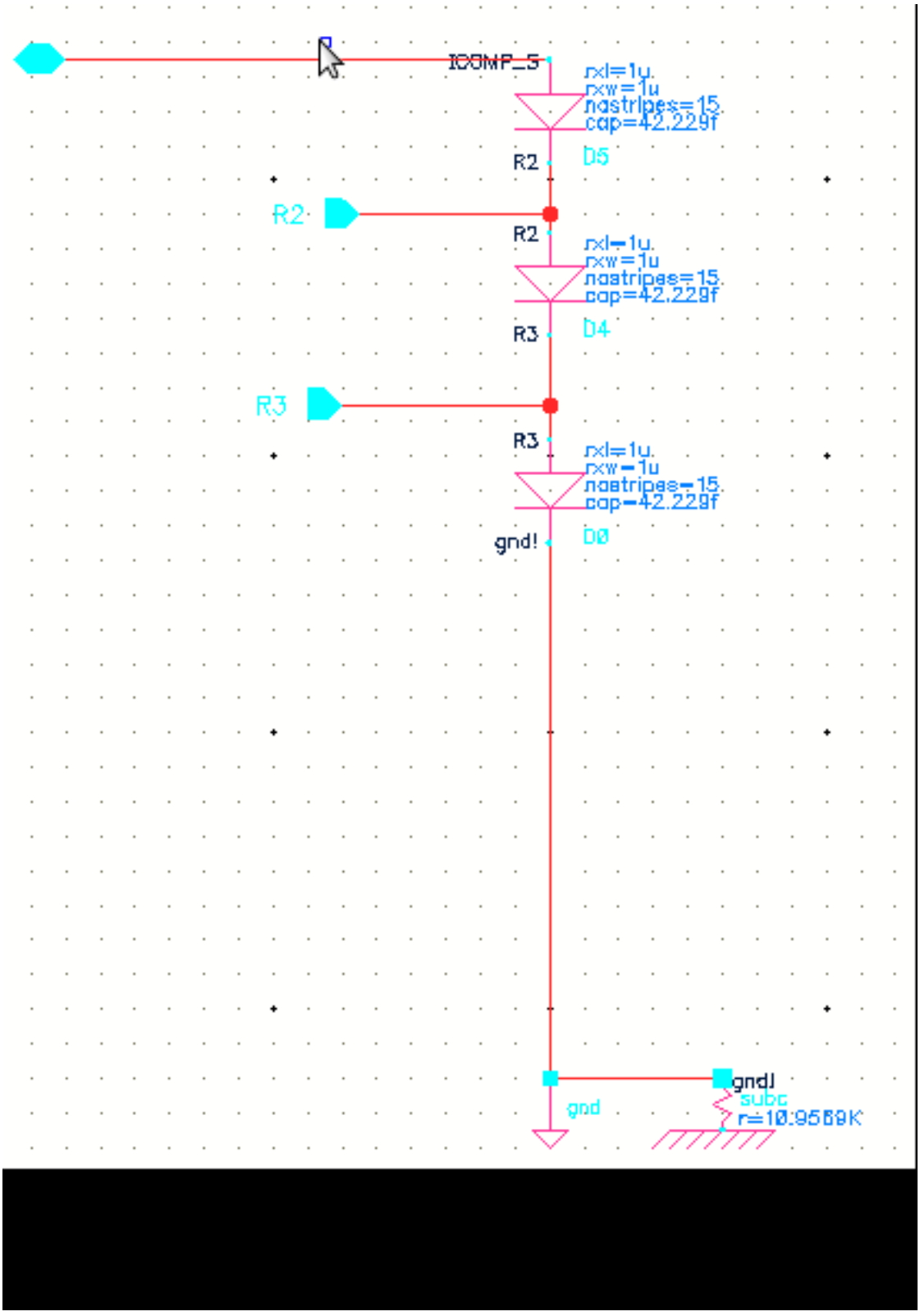

Figure 1.3. Schematic diagram of three diode configuration.

to reach 1.9V is 2.0Ms. For 1mA of input current, the charging time for 100μF capacitor to reach 2.7V is 0.25s and the charging time for 100mF capacitor to reach 2.7V is 250s.

1.3.2 ItoV Converter with four diodes

The four diode configuration generates the voltage of about 2.5V. As mentioned, two ItoV Converter with 100μF and 100mF capacitors across them. The time taken to charge 100mF is higher than 100μF. The schematic and layout diagram of four diode configuration is shown in figure 1.9 and figure 1.10.

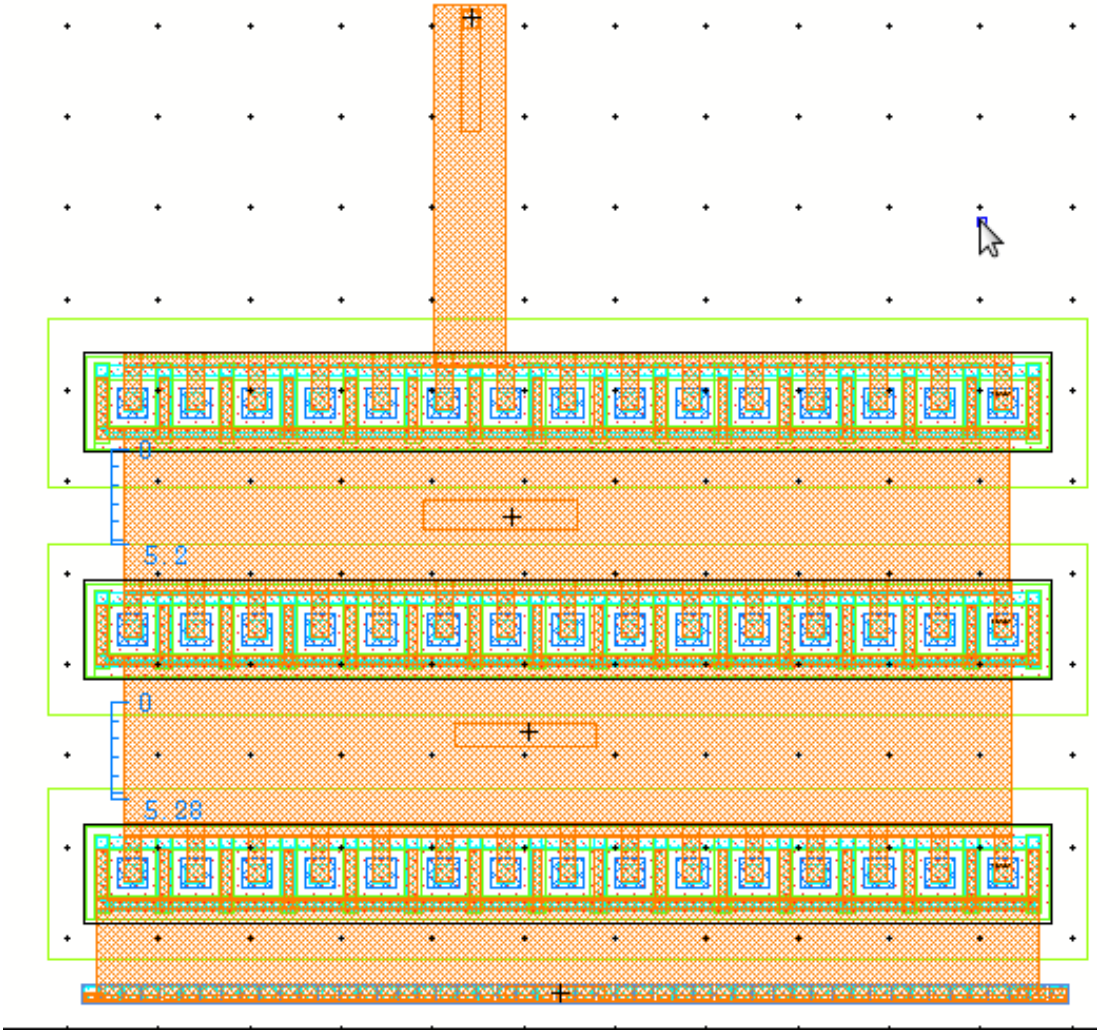

Figure 1.4. Layout of three diode configuration.

The simulation results for four diode ItoV converter configuration for input currents 100nA is also presented in this section. The simulation results for 100nA current is shown in figure 1.12. The charging time for 100μF capacitor to reach 2.5V is 2.8Ks. The charging time for 100mF capacitor to reach 2.5V is 2.8Ms.

1.4 Comparator

The comparator [3] output generates the control voltage to the switch and the working of the comparator is explained in this section.

1.4.1 Hysteresis Comparator

The block diagram of the comparator is shown in figure 1.13.

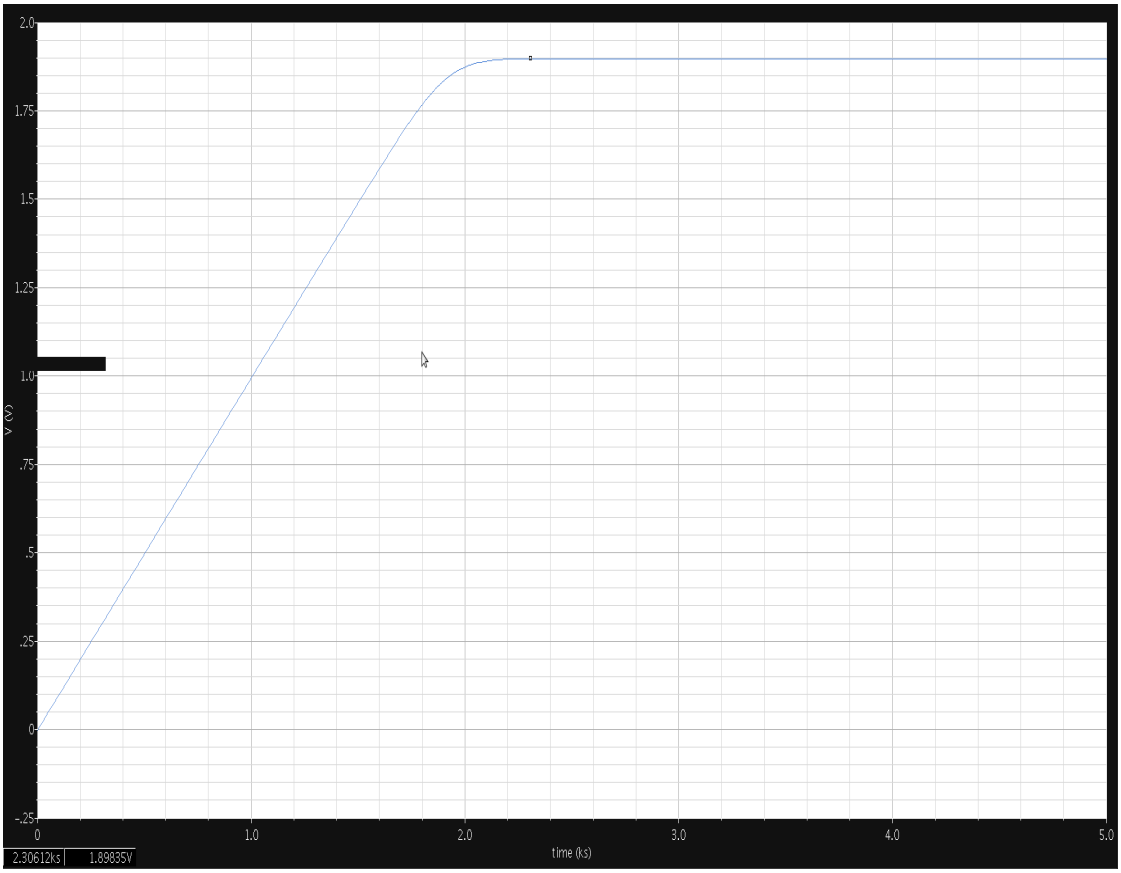

Figure 1.5. Time domain response of Three diode ItoV Converter with 100nA input current and 100μF capacitor across it.

The voltage across 100mF capacitor rises from 0V. When an upper threshold voltage (V_IH) is reached, the comparator becomes active and output of the comparator is high. The comparator output will be high untill the voltage across 100mF capacitor is less than lower threshold (V_{IL}).

The upper and lower hysteresis voltage at the output of the comparator are given by Equation 1.1 and Equation 1.2

$$V_{OH} = V_{DD}\frac{R_2}{R_1 + R_2} - V_{IL} \tag{1.1}$$

$$V_{OL} = V_{DD}\frac{R_2}{R_1 + R_2} - V_{IH} \tag{1.2}$$

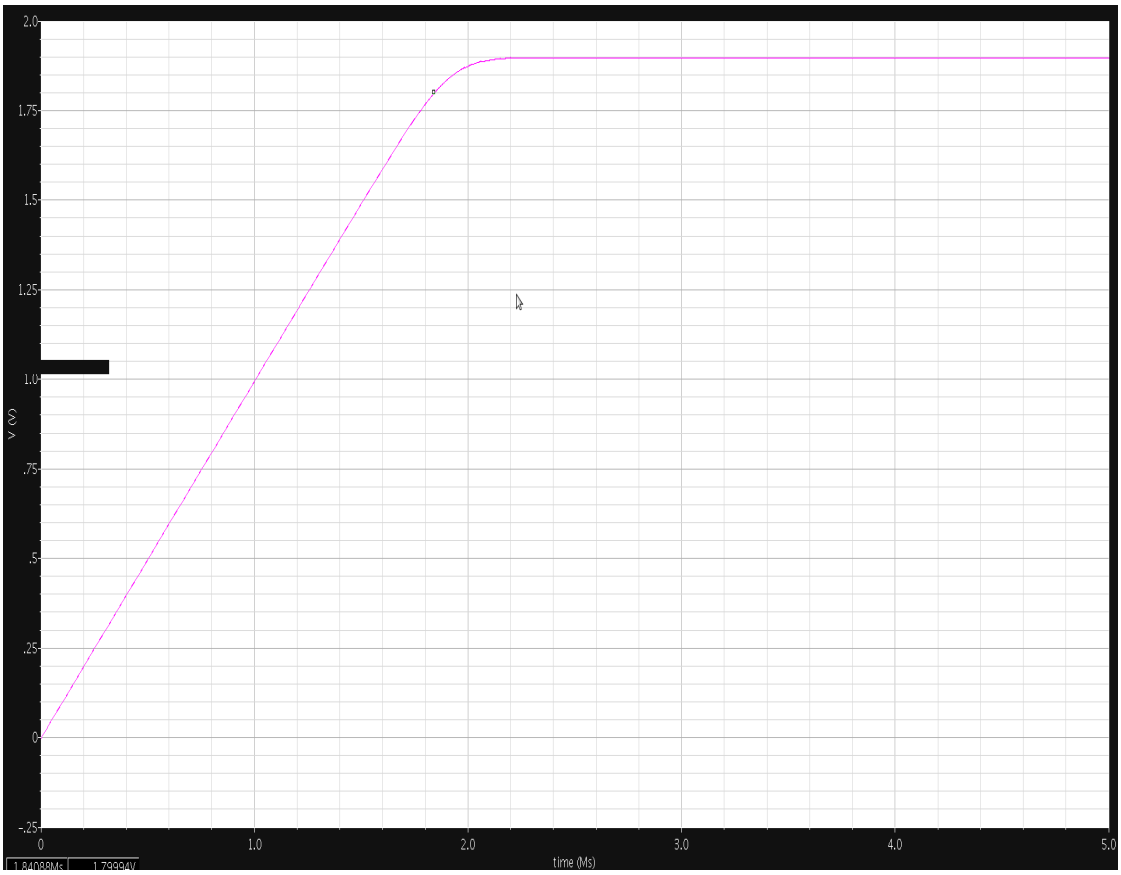

Figure 1.6. Time domain response of Three diode ItoV Converter with 100nA input current and 100mF capacitor across it.

Where V_{IL}, V_{IH}, V_{OL}, V_{OH} and V_{DD} are low input threshold voltage, high input threshold voltage, low output threshold voltage, high output threshold voltage and supply voltage for comparator.

The schematic and layout of the Hysteresis comparator are shown in figure 1.14 and figure 1.15.

The time domain simulation results of comparator for three diode configurations are shown in figure 1.16 and figure 1.17.

The hysteresis response of the comparator for 1.8V and 2.7V supply voltage is shown in figure 1.18 and figure 1.19

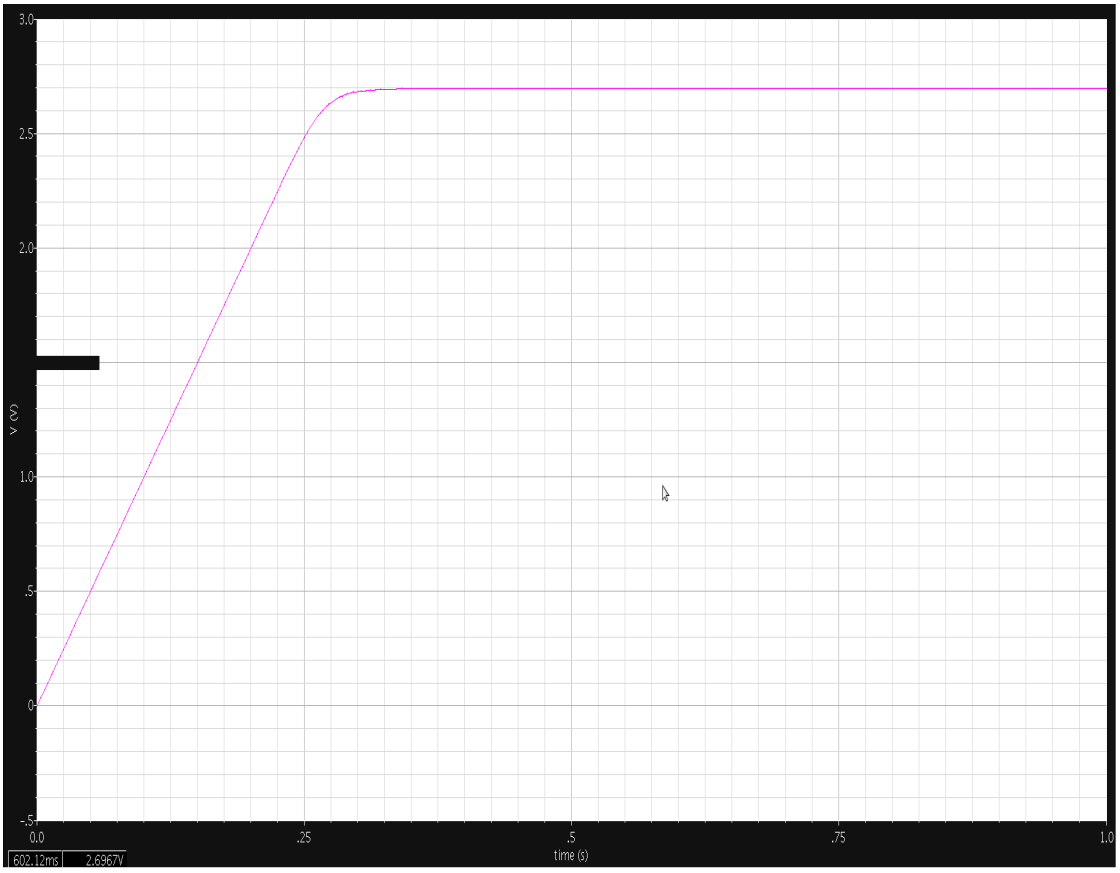

Figure 1.7. Time domain response of Three diode ItoV Converter with 1mA input current and 100μF capacitor across it.

The output of the comparator is around 1.8V when input voltage varies from 1.55V to 1.75V. The output of the comparator is around 2.7V when input voltage varies from 2.4V to 2.65V.

1.5 Switch

The switch is pass transistor designed with PMOS. The width of the switch is approximately 1mm to drive the maximum current to the output. The schematic of the switch configuration is shown in figure 1.20.

The source of the switch is connected to ItoV Converter with 100mF capacitor and the drain of the switch is connected to the functional design. The gate control voltage is generated by the comparator.

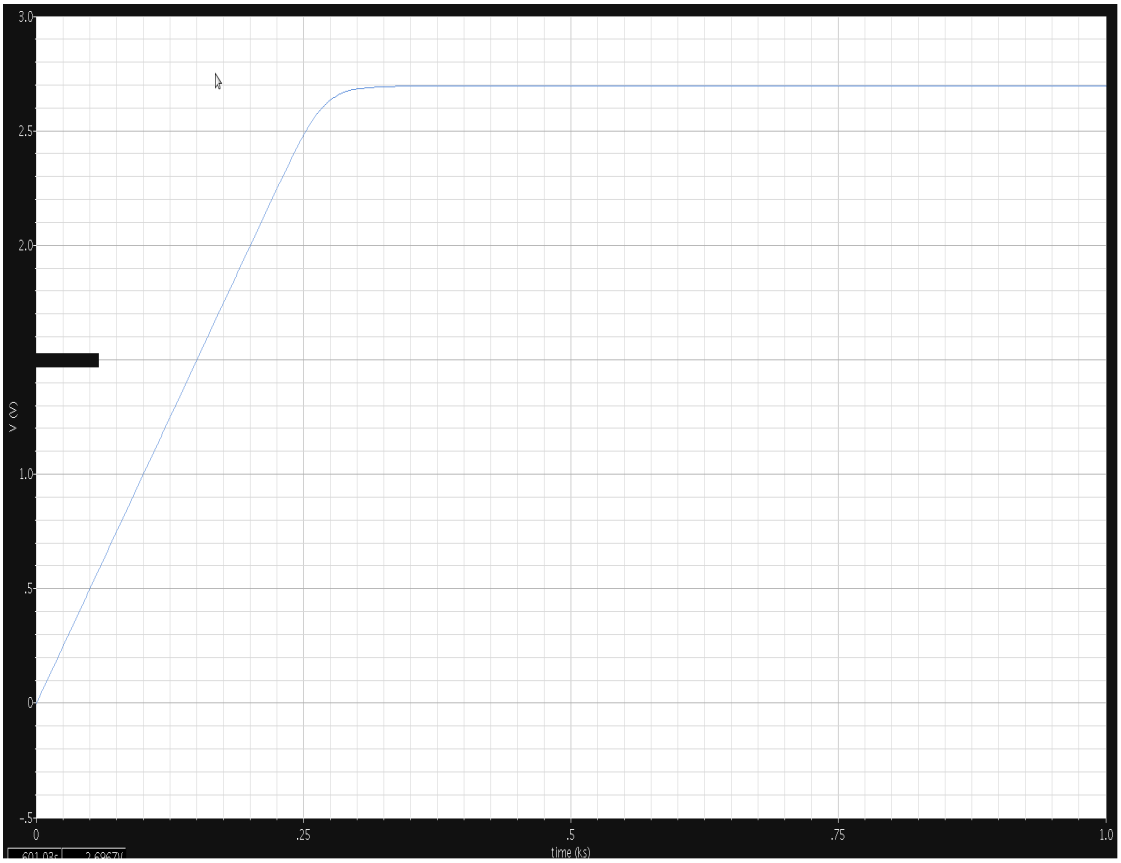

Figure 1.8. Time domain response of Three diode ItoV Converter with 100nA input current and 100mF capacitor across it.

When the gate control voltage is high, the charge stored across 100mF capacitor discharges to functional design. When the charge across the 100mF capacitor falls below lower threshold (V_{IL}), the comparator output generates zero voltage and the switch is in OFF position via an inverter. Then the 100mF capacitor charges till the voltage across it reaches higher threshold (V_{IH}) value. This again activates the comparator circuit and switches on the PMOS circuit via an inverter.

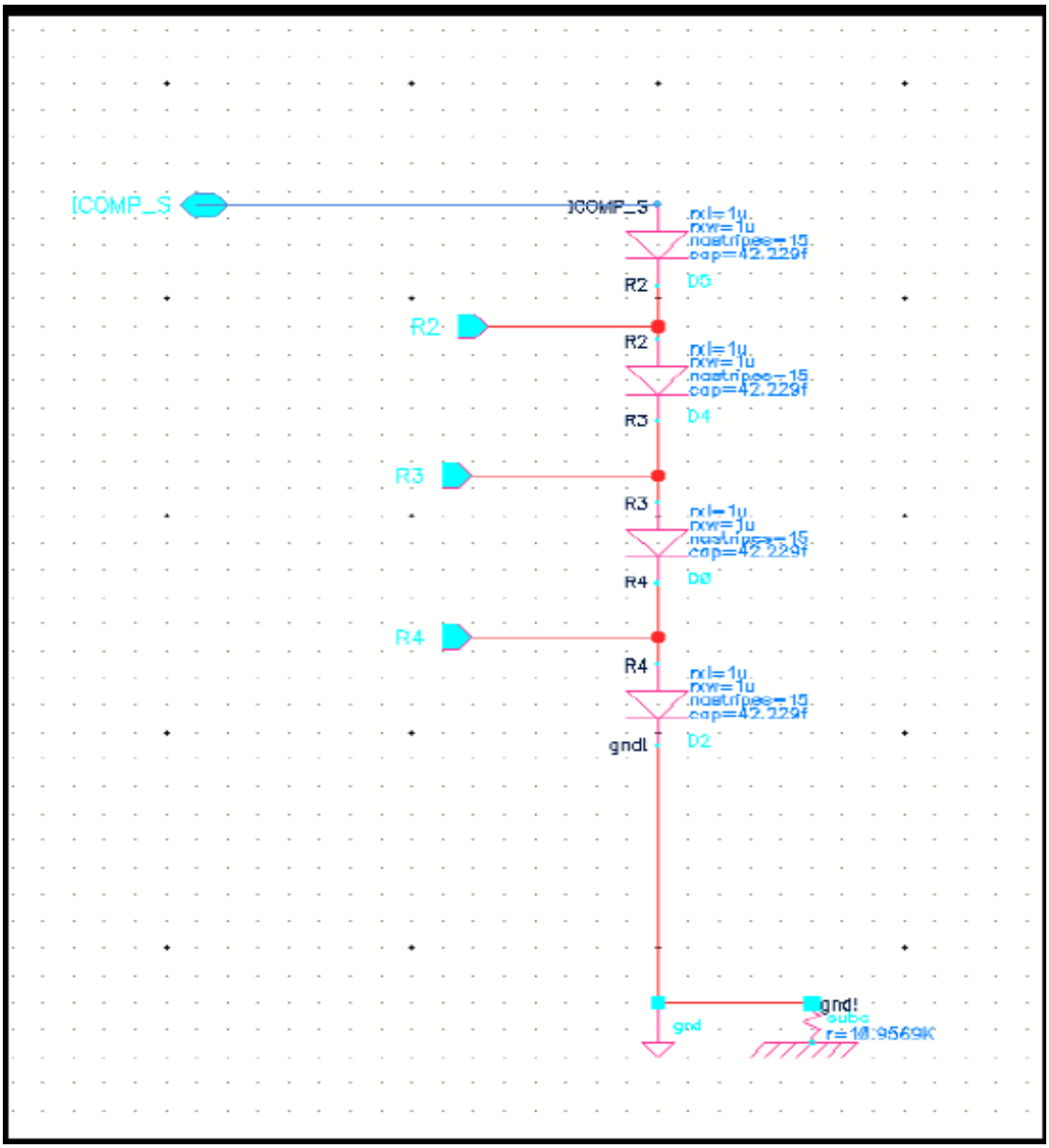

Figure 1.9. Schematic diagram of four diode configuration.

The layout of the implemented design with three diodes and four diodes are shown in figure 1.21 and figure 1.22.

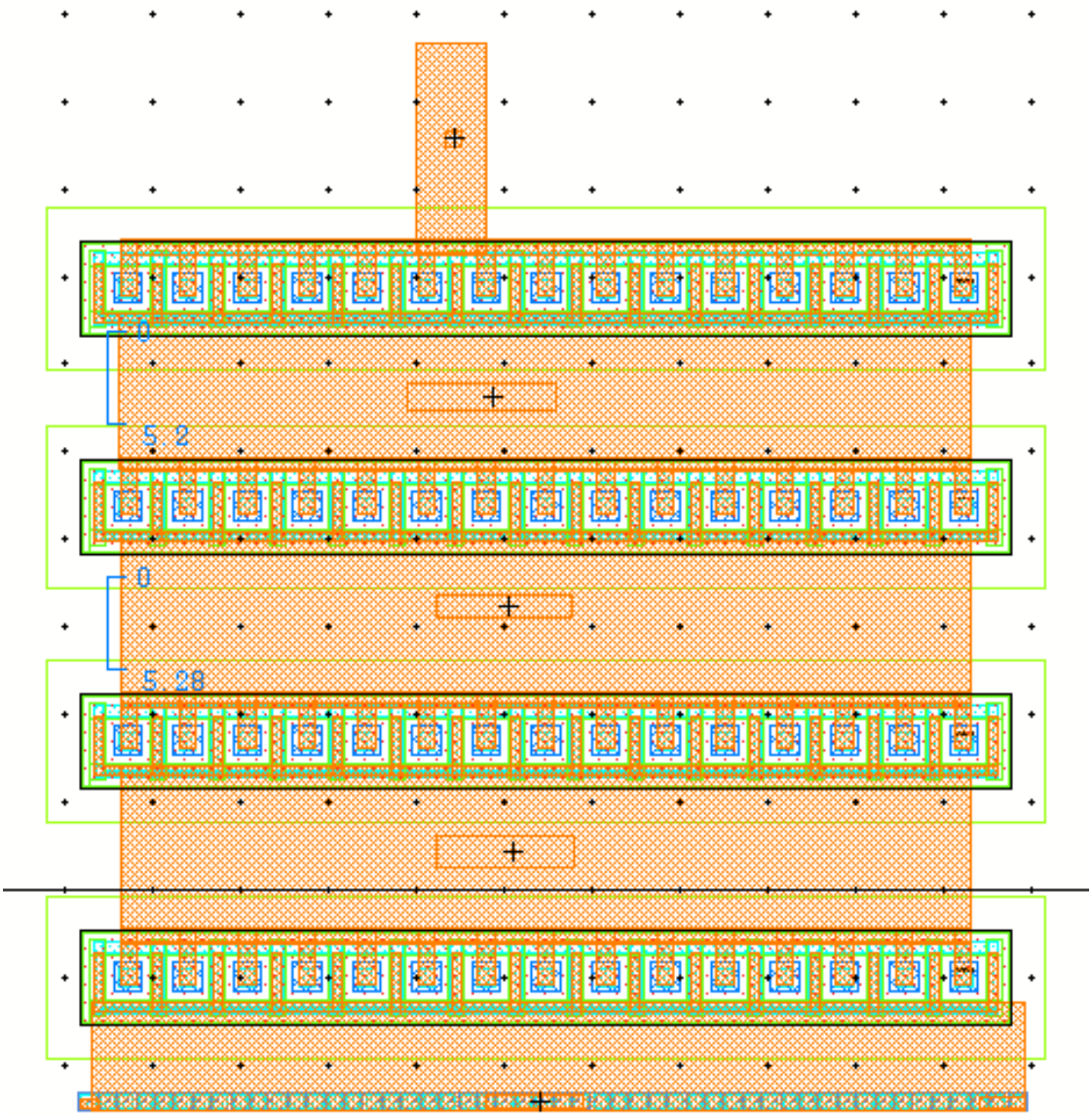

Figure 1.10. Layout of four diode configuration.

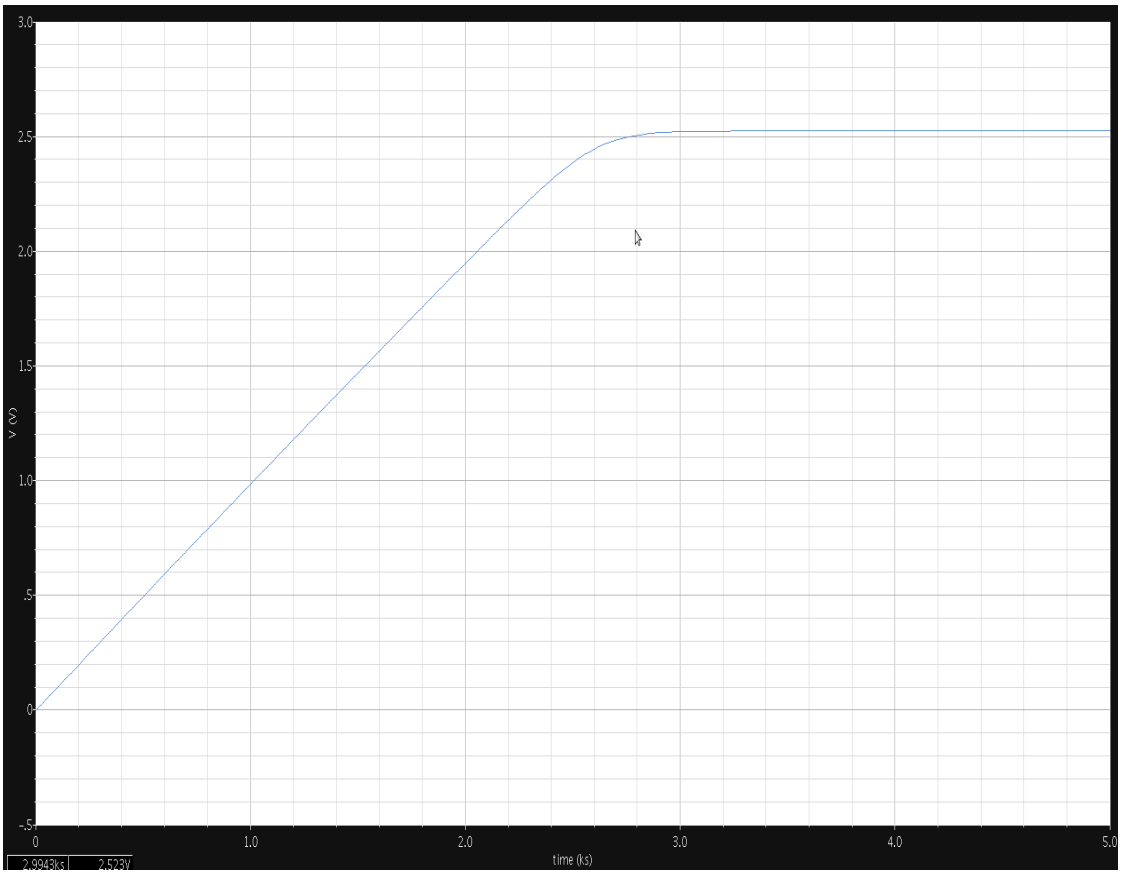

Figure 1.11. Time domain response of Four diode ItoV Converter with 100nA input current and 100μF capacitor across it.

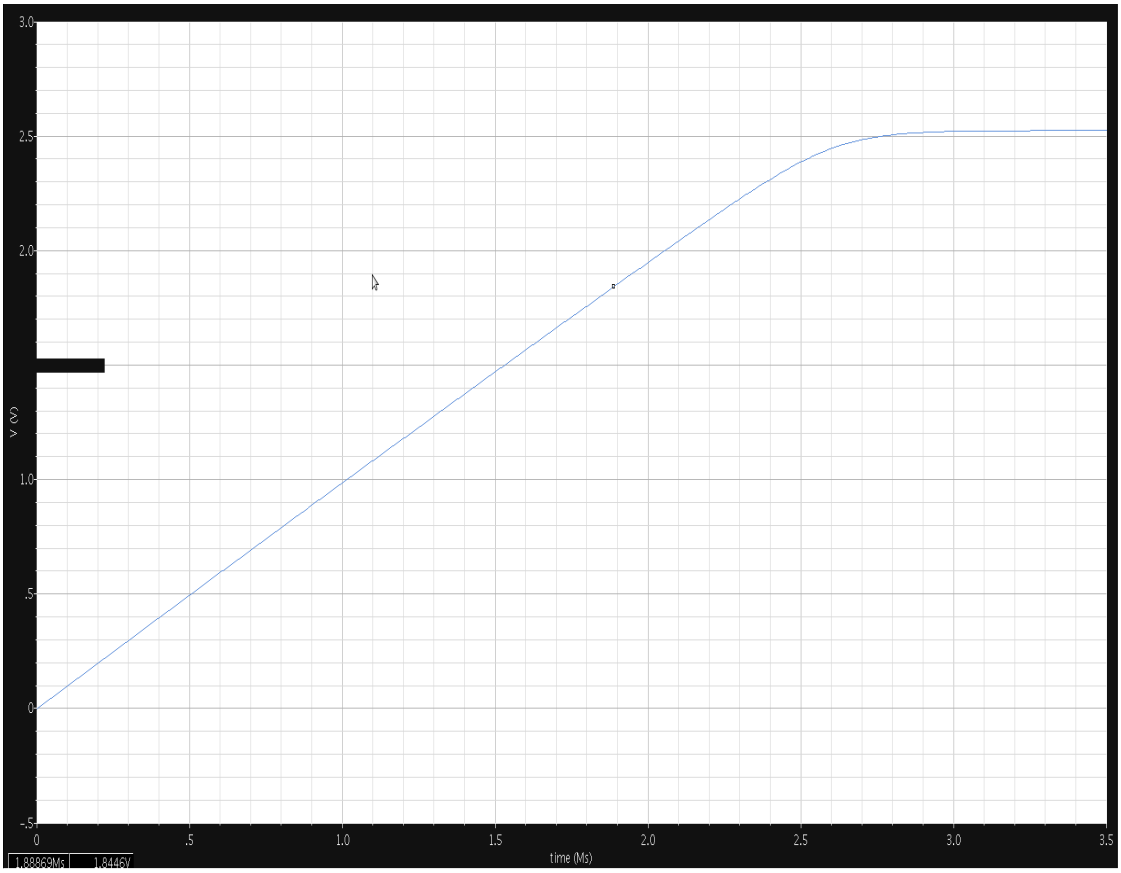

Figure 1.12. Time domain response of Four diode ItoV Converter with 100nA input current and 100mF capacitor across it.

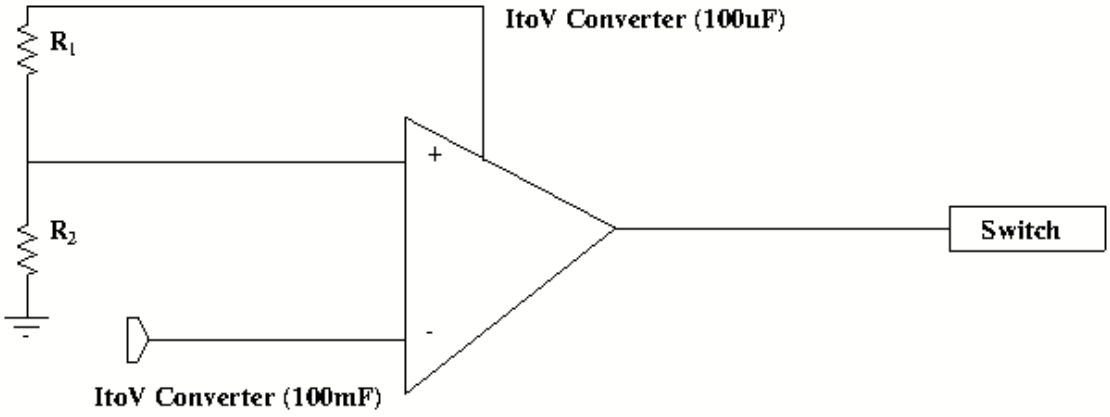

Figure 1.13. Block diagram of Hysteresis Comparator.

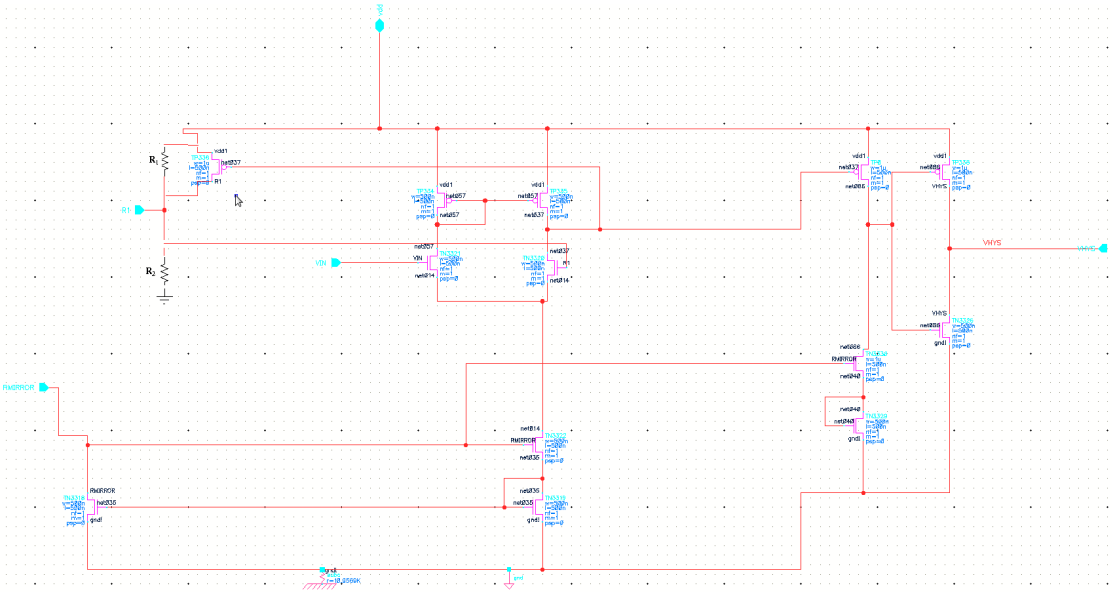

Figure 1.14. Schematic of Hysteresis Comparator.

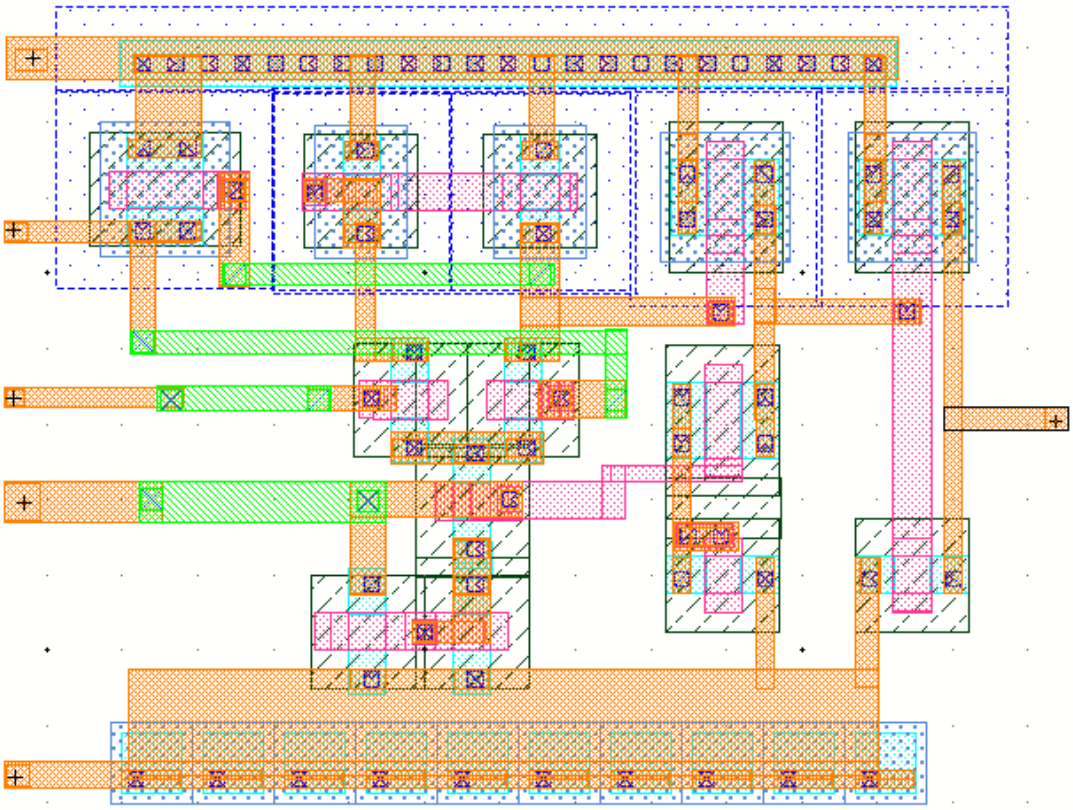

Figure 1.15. Layout of Hysteresis Comparator.

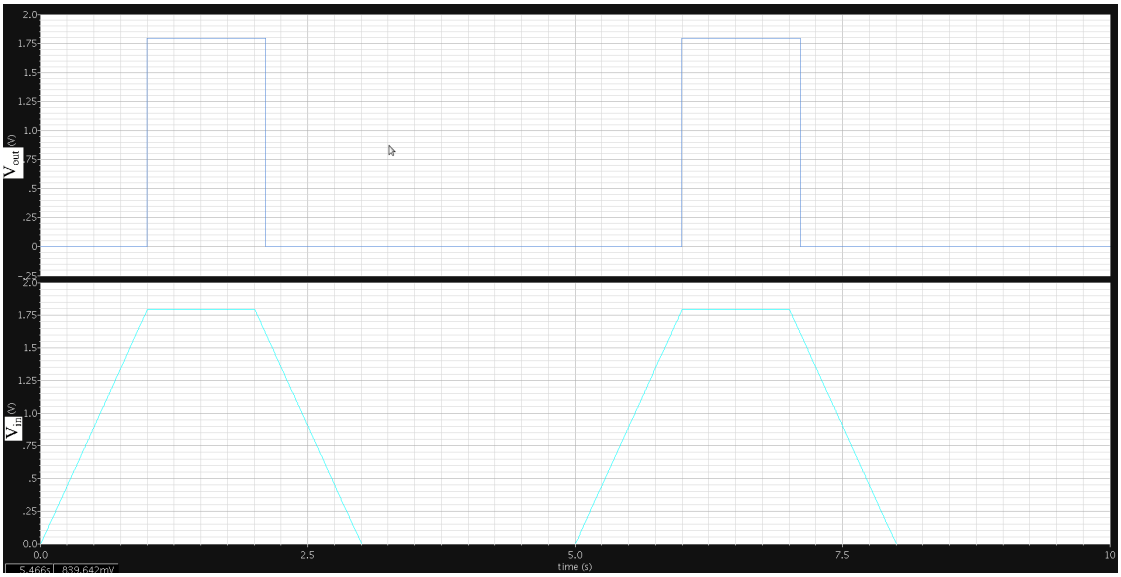

Figure 1.16. Time domain response of comparator for 1.8V supply voltage

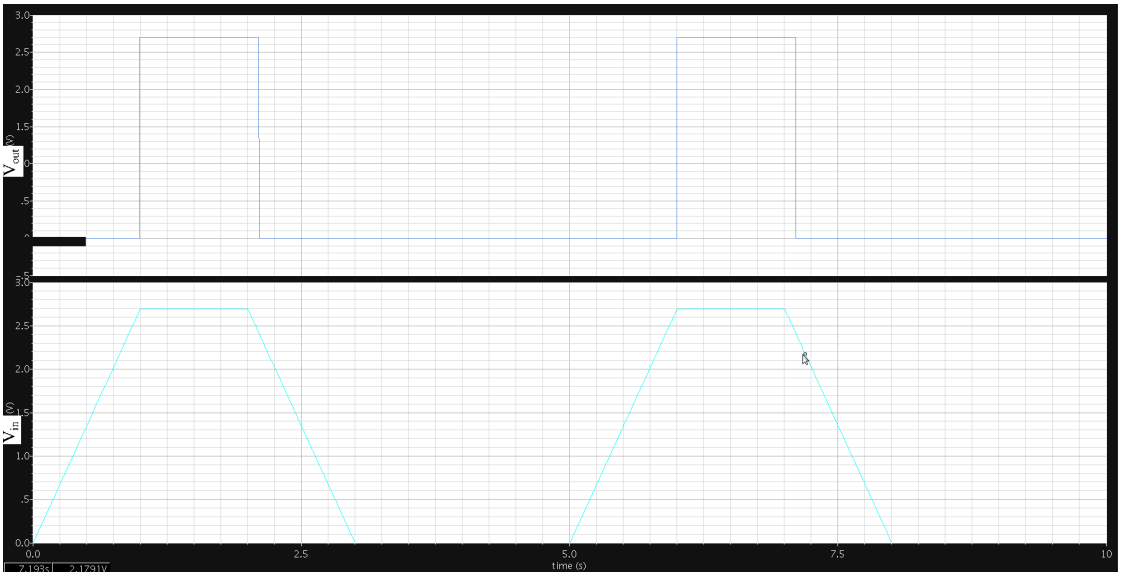

Figure 1.17. Time domain response of comparator for 2.7V supply voltage

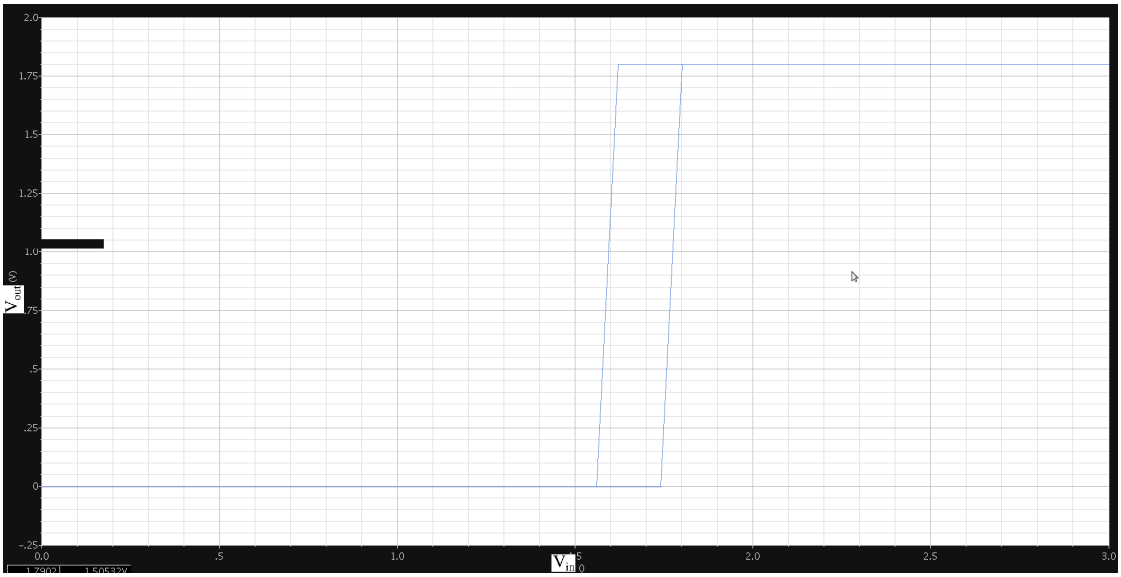

Figure 1.18. Hysteresis response of comparator for 1.8V supply voltage.

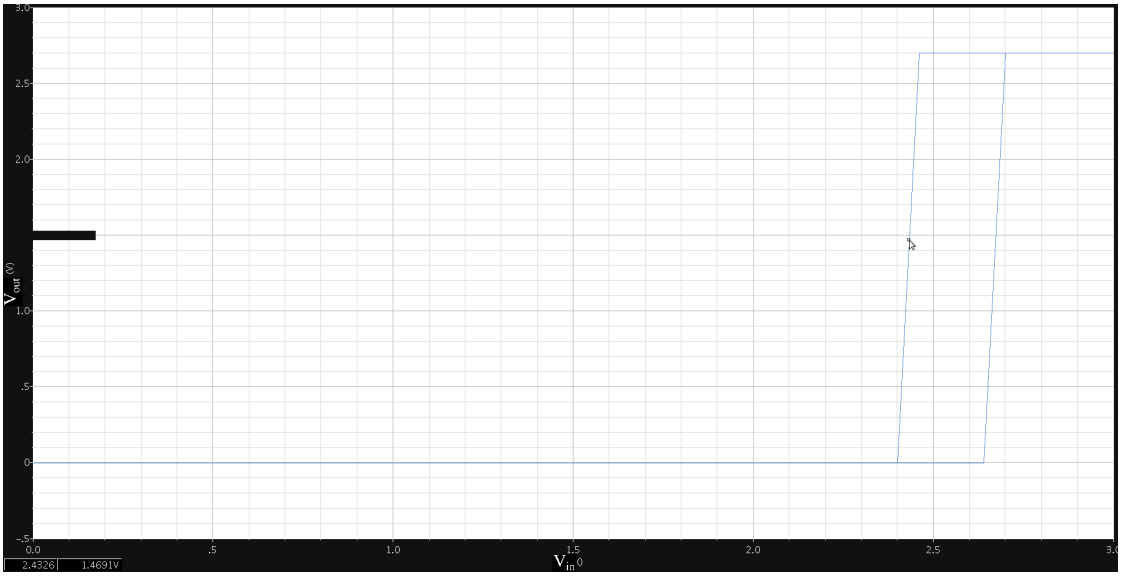

Figure 1.19. Hysteresis response of comparator for 2.7V supply voltage

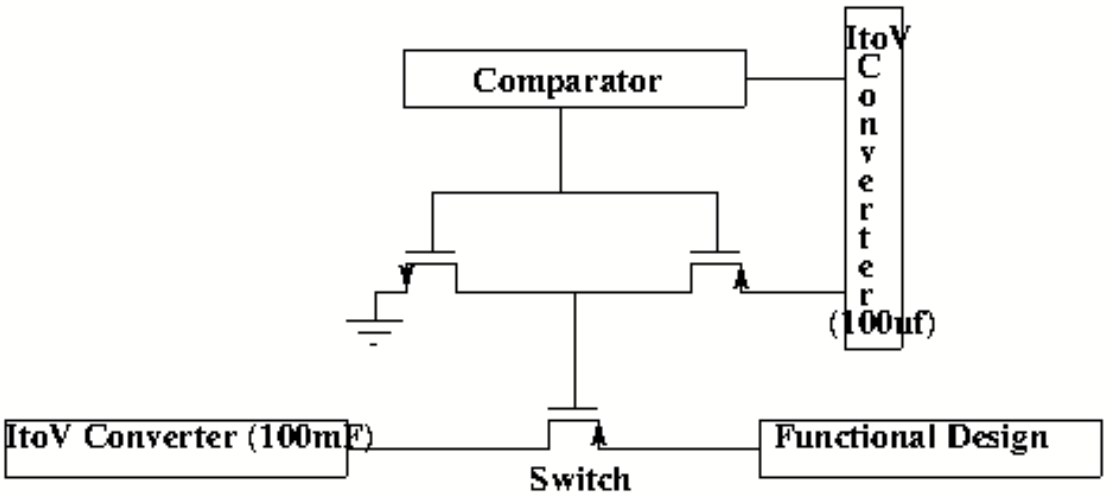

Figure 1.20. The switch configuration of the EMS.

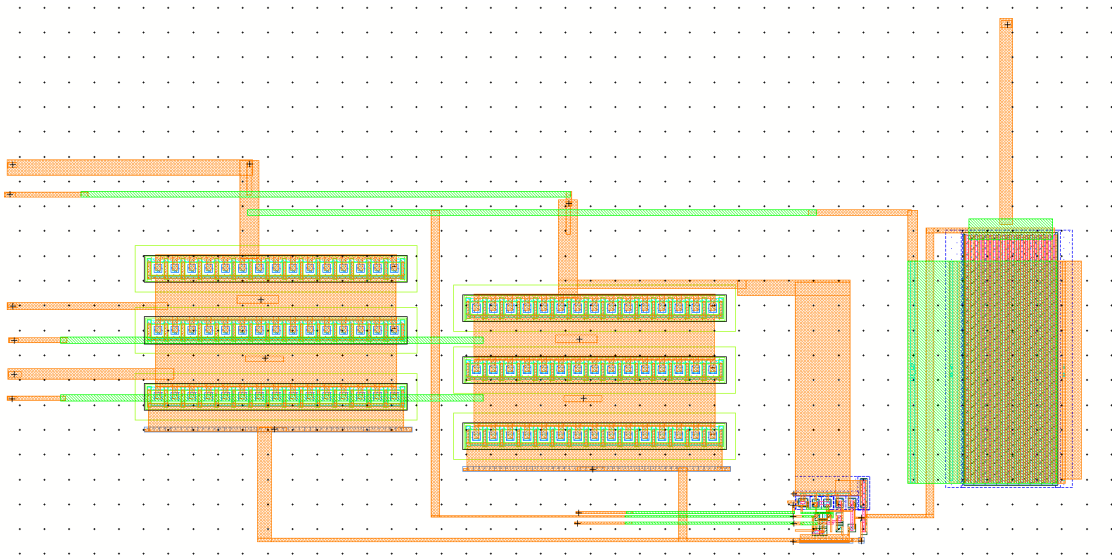

Figure 1.21. The layout of the EMS with three diode configuration.

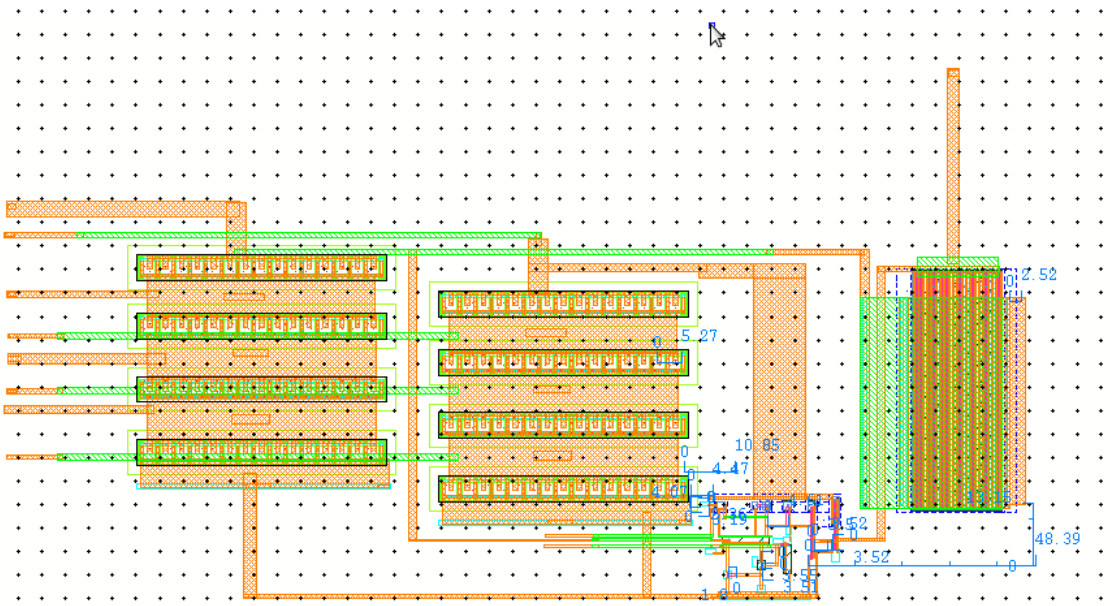

Figure 1.22. The layout of the EMS with four diode configuration.

Chapter 2

Simulation Results and Test Procedures

This chapter gives the details of the simulation results of EMS and chip. The design is implemented in Dual In Packaged (DIP) chip with 40 pins. The total area of the chip is 1.5mm X 1.5mm with Electro Static Discharge (ESD) diodes for protection. The chip consists of four EMS designs :

1. Three with three diode configuration (Circuit1 and Circuit2).

2. one with four diode configuration (Circuit3 and Circuit4).

The schematic and layout of the EMS is shown in figure 2.1 and figure 2.2.

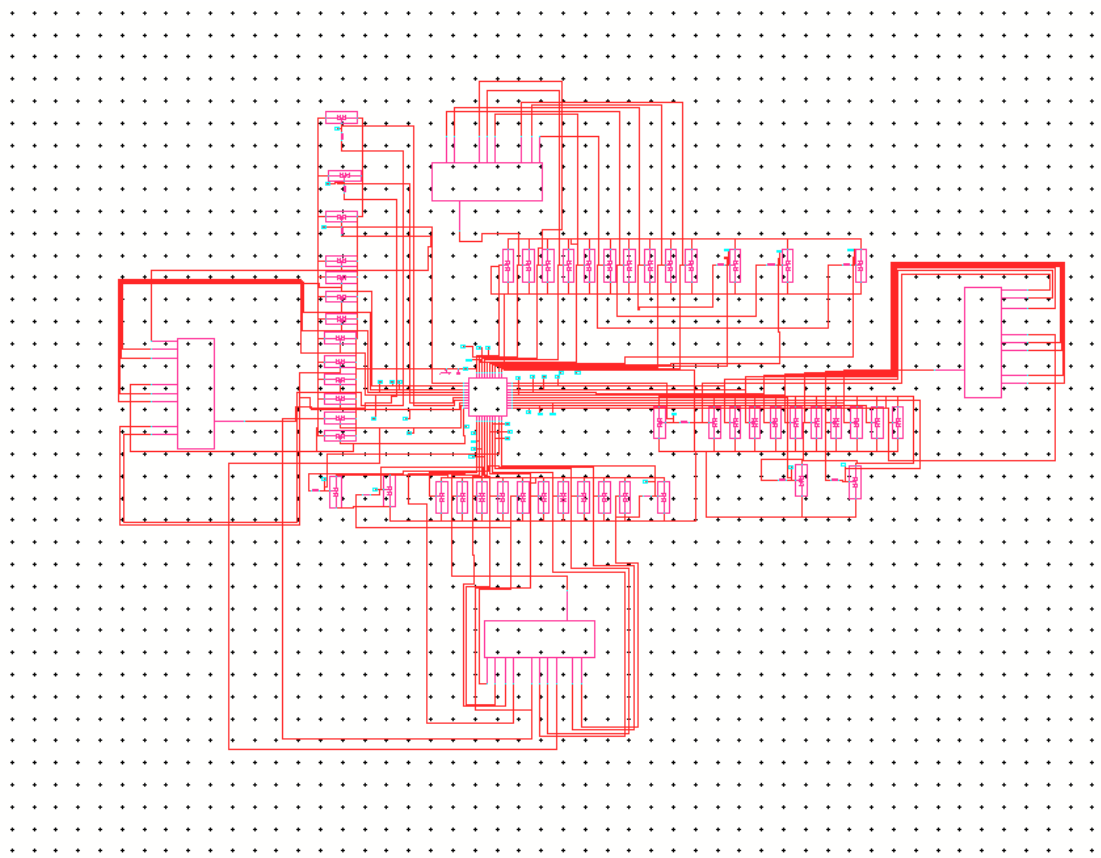

Figure 2.1. Schematic of the chip with four EMS designs inside.

2.1 Simulation Results

The simulation results for three diode ItoV Converter configuration with 100nA and 1mA input currents are shown in figure 2.3 and figure 2.4.

The simulation results for four diode ItoV Converter configuration with 100nA input current is shown in figure 2.5.

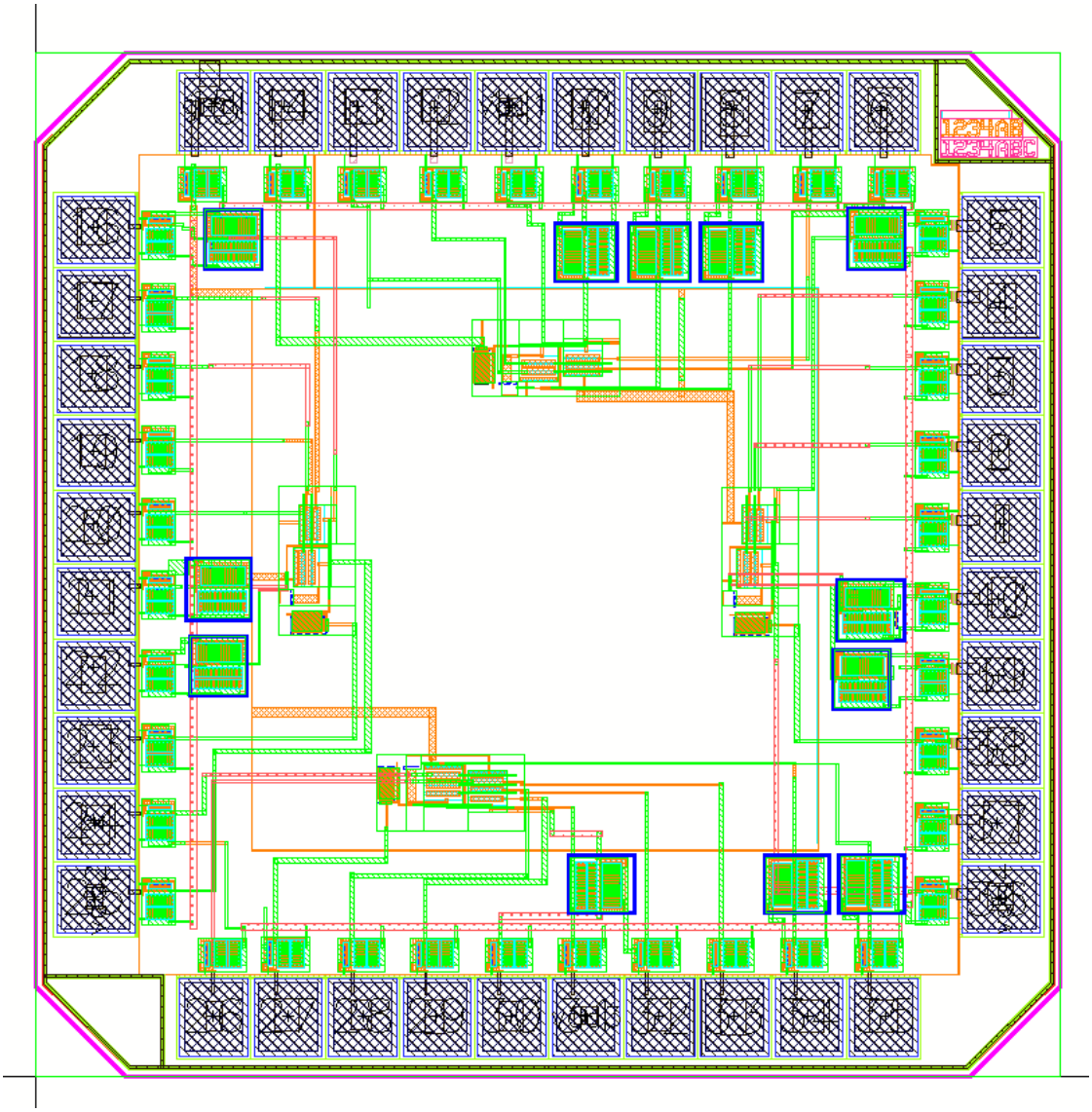

Figure 2.2. Layout of the chip with four EMS designs inside.

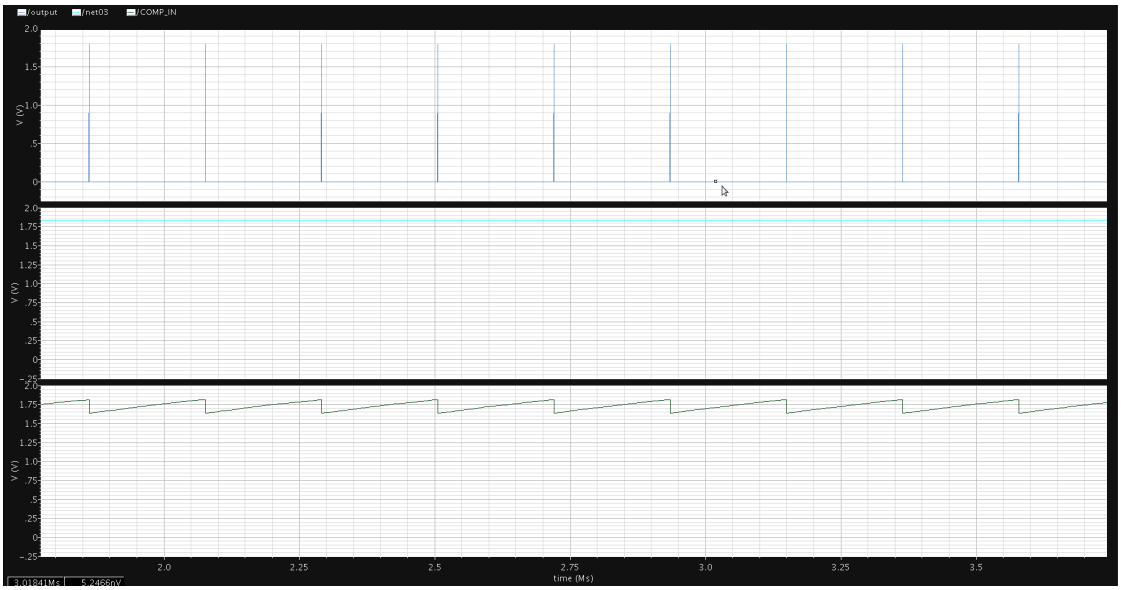

Figure 2.3. Time domain response of comparator supply voltage (middle), input of comparator (bottom) and output of EMS (top).

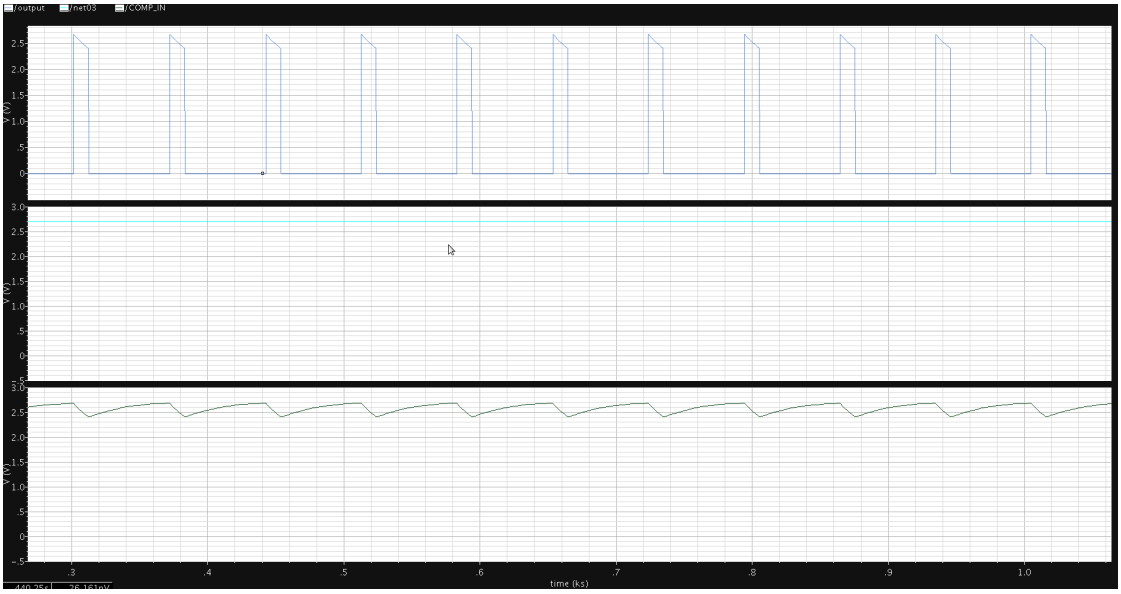

Figure 2.4. Time domain response of comparator supply voltage (middle), input of comparator (bottom) and output of EMS (top) .

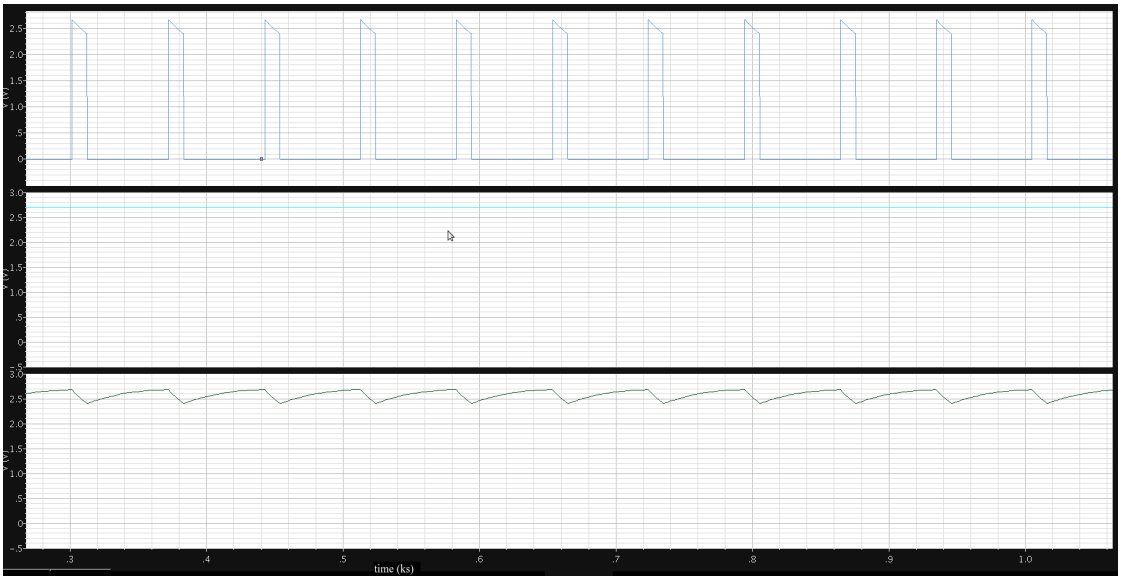

Figure 2.5. Time domain response of comparator supply voltage (middle), input of comparator (bottom) and output of EMS (top) .

2.2 Pin configurations in the design

2.2.1 Circuit1

1. Connect 100 MΩ resistors between 10 and 7, 7 and 6, 6 and 15, 11 and 12, 12 and 13 and 13 and 15.

2. Connect 120 to 150 MΩ resistor between 11 and 8.Place a 20 MΩ resistor between 11 and 9 and 100 Mohms between 9 and 15.

3. Place a 100μF and a current source capacitor between 11 and 15. A current source and 100mF capacitor is placed between 10 and 15.

4. Finally a 800Ω resistor is placed between 14 and 15 to verify the output.

2.2.2 Circuit2

1. Connect 100 MΩ resistors between 16 and 17, 17 and 18, 18 and 15, 25 and 19, 19 and 20 and 20 and 15.

2. Connect 120 to 150 MΩ resistor between 25 and 21.Place a 20 MΩ resistor between 25 and 22 and 100 MΩ between 22 and 15.

3. Place a 100μF and a current source capacitor between 25 and 15. A current source and 100mF capacitor is placed between 16 and 15.

4. Finally a 800Ω resistor is placed between 23 and 15 to verify the output.

2.2.3 Circuit3

1. Connect 100 MΩ resistors between 36 and 2, 2 and 1, 1 and 15, 5 and 4, 4 and 3 and 3 and 15.

2. Connect 120 to 150 MΩ resistor between 36 and 40. Place a 20 MΩ resistor between 36 and 39 and 100 MΩ between 39 and 15.

3. Place a 100μF and a current source capacitor between 36 and 15. A current source and 100mF capacitor is placed between 5 and 15.

4. Finally a 800Ω resistor is placed between 38 and 15 to verify the output.

2.2.4 Circuit4

1. Connect 100 MΩ resistors between 31 and 32, 32 and 33, 33 and 24, 24 and 15, 30 and 29, 29 and 28, 28 and 26, and 26 and 15.

2. Connect 120 to 150 MΩ resistor between 31 and 34.Place a 20 MΩ resistor between 31 and 35 and 100 MΩ between 35 and 15.

3. Place a 100μF and a current source capacitor between 31 and 15. A current source and 100mF capacitor is placed between 30 and 15.

4. Finally a 800Ω resistor is placed between 27 and 15 to verify the output.

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REFERENCES

[1] J. Record, "RF Energy Harvesting Circuits," 2011, Available : http://ece.umaine.edu/research/vlsi/student-integrated-circuit-designs/record/.

[2] J. Reinhold, "Low Power Morse Code ROM and and Transmitter for 70cm ISM Band," 2011, Available : http://ece.umaine.edu/research/vlsi/student-integrated-circuit-designs/reinhold/.

[3] P. Allen and D. Holberg, *CMOS Analog Circuit Design*. Oxford series in Electrical and Computer Engineering, Oxford University Press, 2002.

BIOGRAPHY OF THE AUTHOR

Praveen Gunturi was born in India on December 25, 1983. He entered the Jawaharlal Nehru Technological University and obtained his Bachelor of Technology degree in Electronics and Communications Engineering in 2006.

In August 2007, he was enrolled for graduate study in Electronics and Communications Engineering at the National Institute of Technology, Trichy (NITT), India and served as Research Assistant. He majored in Very Large Scale Integrated circuits (VLSI) from NITT.

He secured 450 rank among 30,000 students in Graduate Aptitude Test for Engineering (GATE) 2007 examination in india. He is a student member of IEEE, Marketing Chair for National Society of Black Engineers (NSBE) and Graduate School Government Senator at University of Maine. He served as Placement Representative in NITT.

He is a candidate for the Doctor of Philosophy degree in Electrical and Computer Engineering from the University of Maine from Jan 2011. His current research interests include Ultra WideBand (UWB) and Power Amplifiers (PA).