

VLSI Design and Test of Digital Phase-Locked Loops

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Introduction

My project is to design Digital Phase-Locked Loops (DPLL) in a DIP40 chip.

I implement two sets of DPLL in the chip: one is for input data frequency about 20MHz, and the other is for 25MHz.

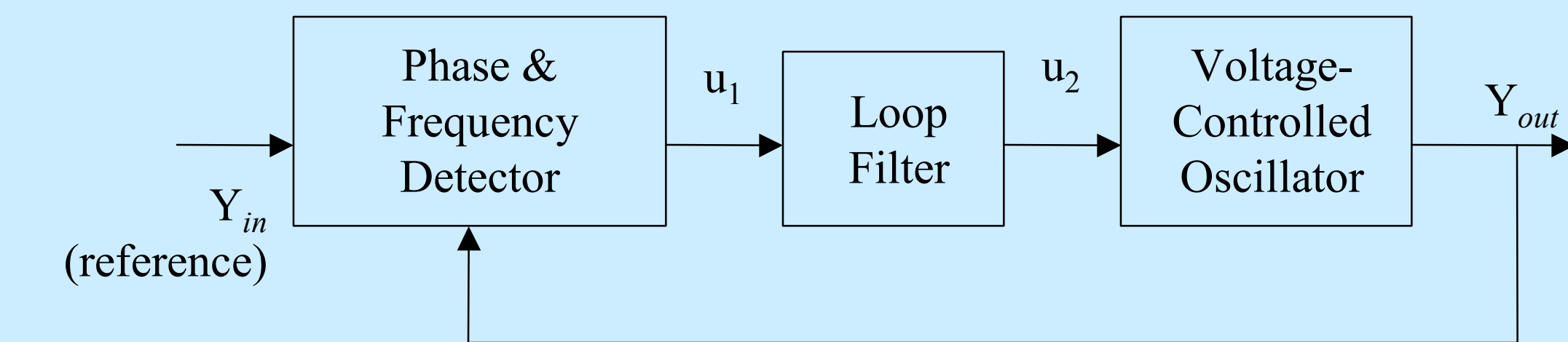


Figure 1. Block of PLL

PLL has three major components: Phase and Frequency Detector (PFD), Loop Filter and Voltage-Controlled Oscillator (VCO).

PLL synchronizes the VCO to the input signal (reference).

Phase Detector compares the reference input to the VCO's output and produces a signal u_1 .

Loop Filter processes u_1 to provide the oscillator control signal u_2 .

VCO's frequency changes in response to u_2 .

Design of Schematic and Layout

The platform I used to design and simulate the schematic and layout is Cadence.

• Phase & Frequency Detector

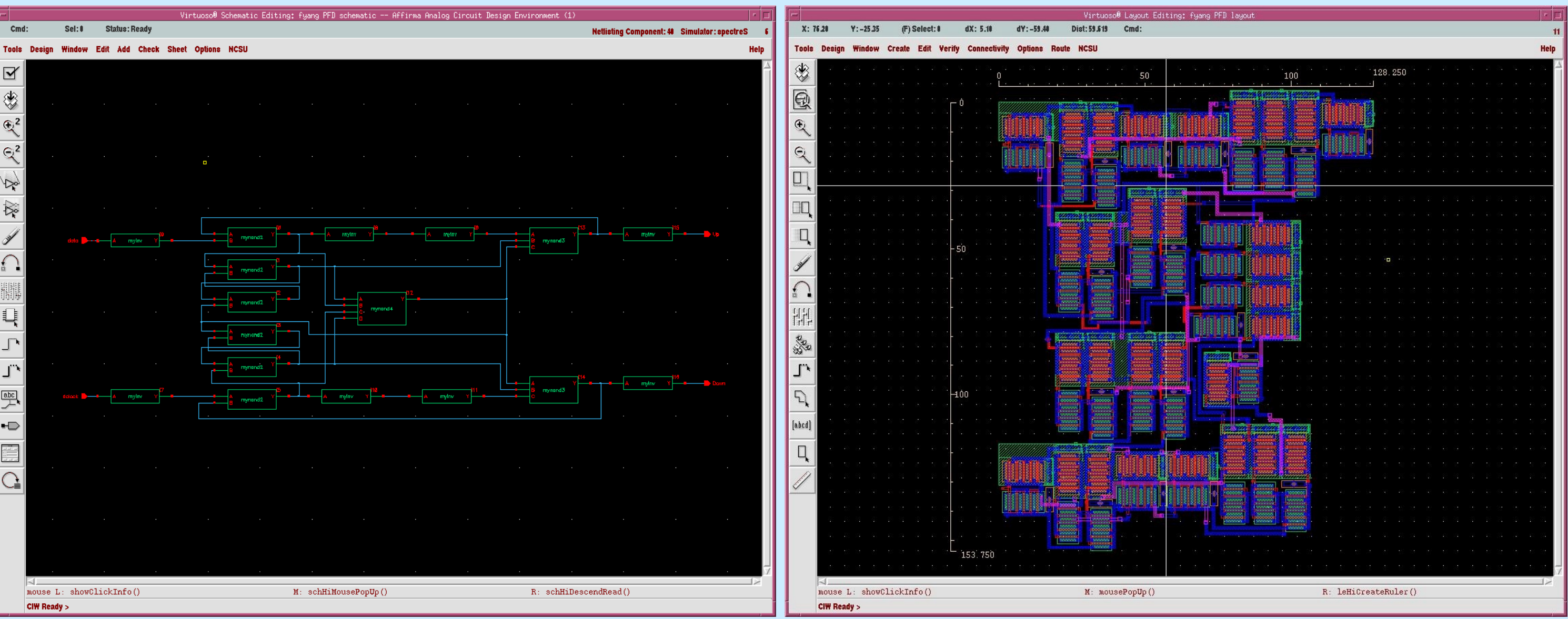


Figure 2. Schematic of PFD

Figure 3. Layout of PFD

• Voltage-Controlled Oscillator



Figure 4. Schematic of Voltage-Controlled Oscillator

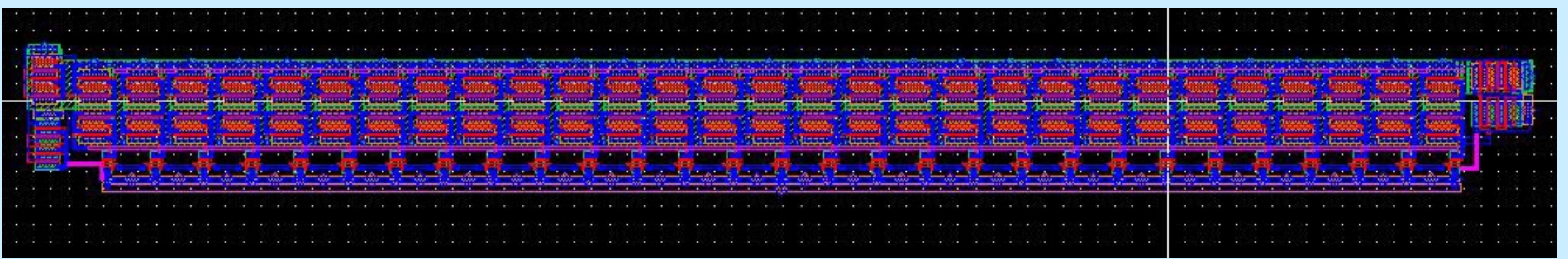


Figure 5. Layout of Voltage-Controlled Oscillator

• Loop Filter (Charge Pump and RC filter)

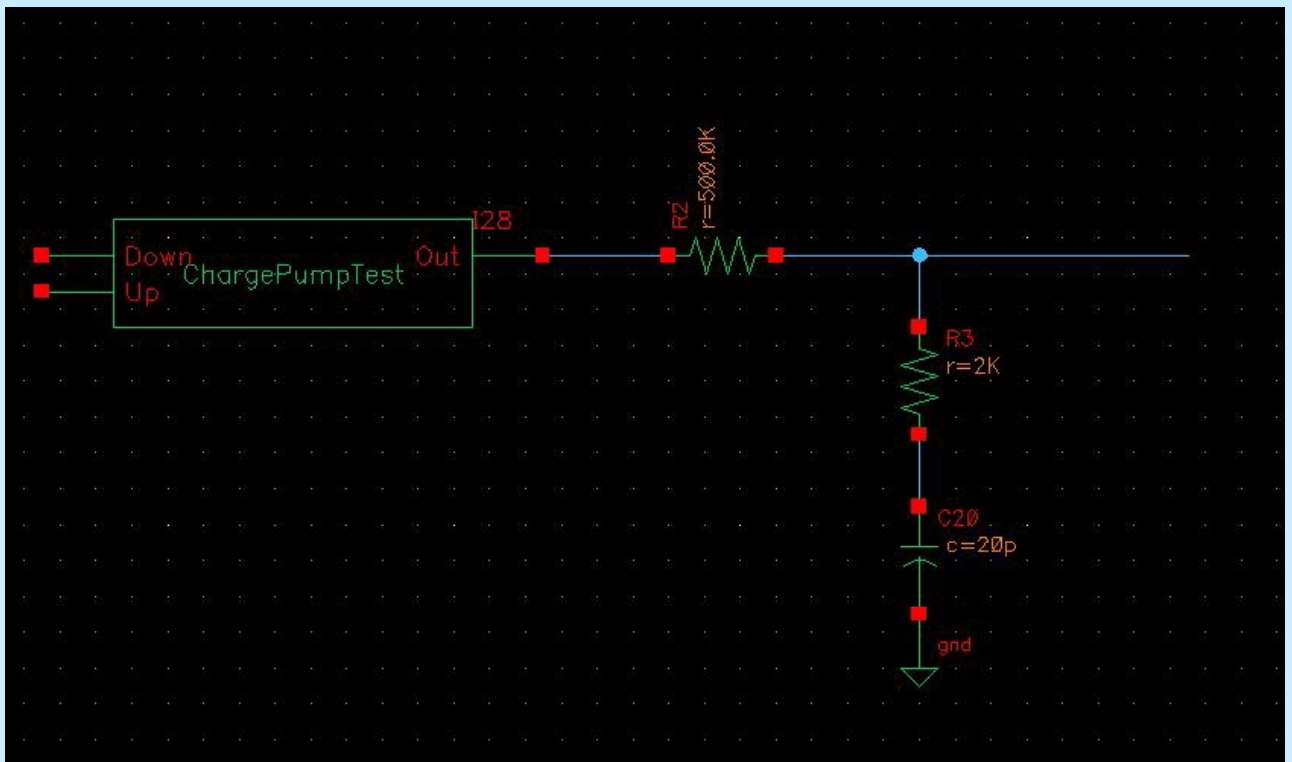


Figure 6. Schematic of Loop Filter

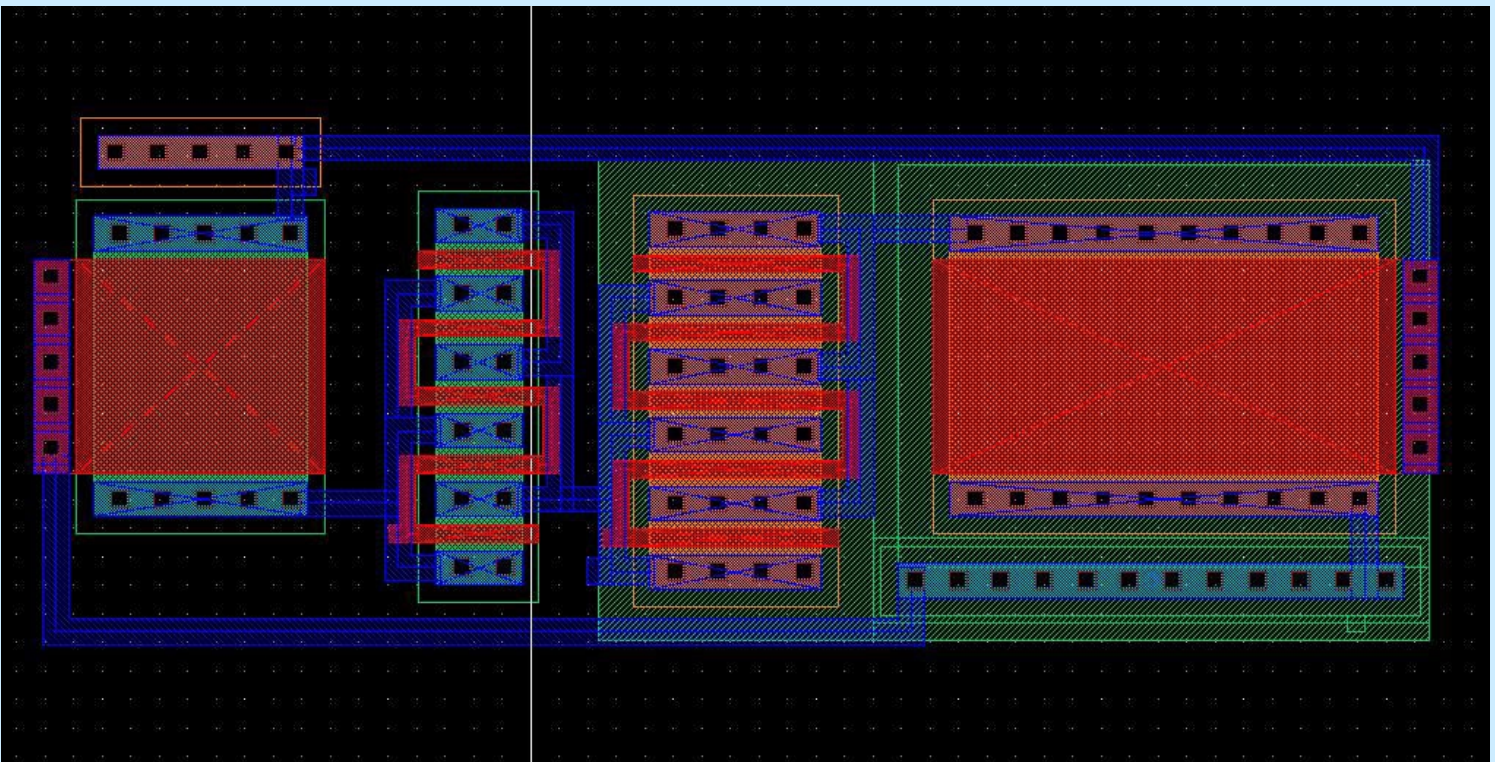


Figure 7. Layout of Charge Pump

Simulation

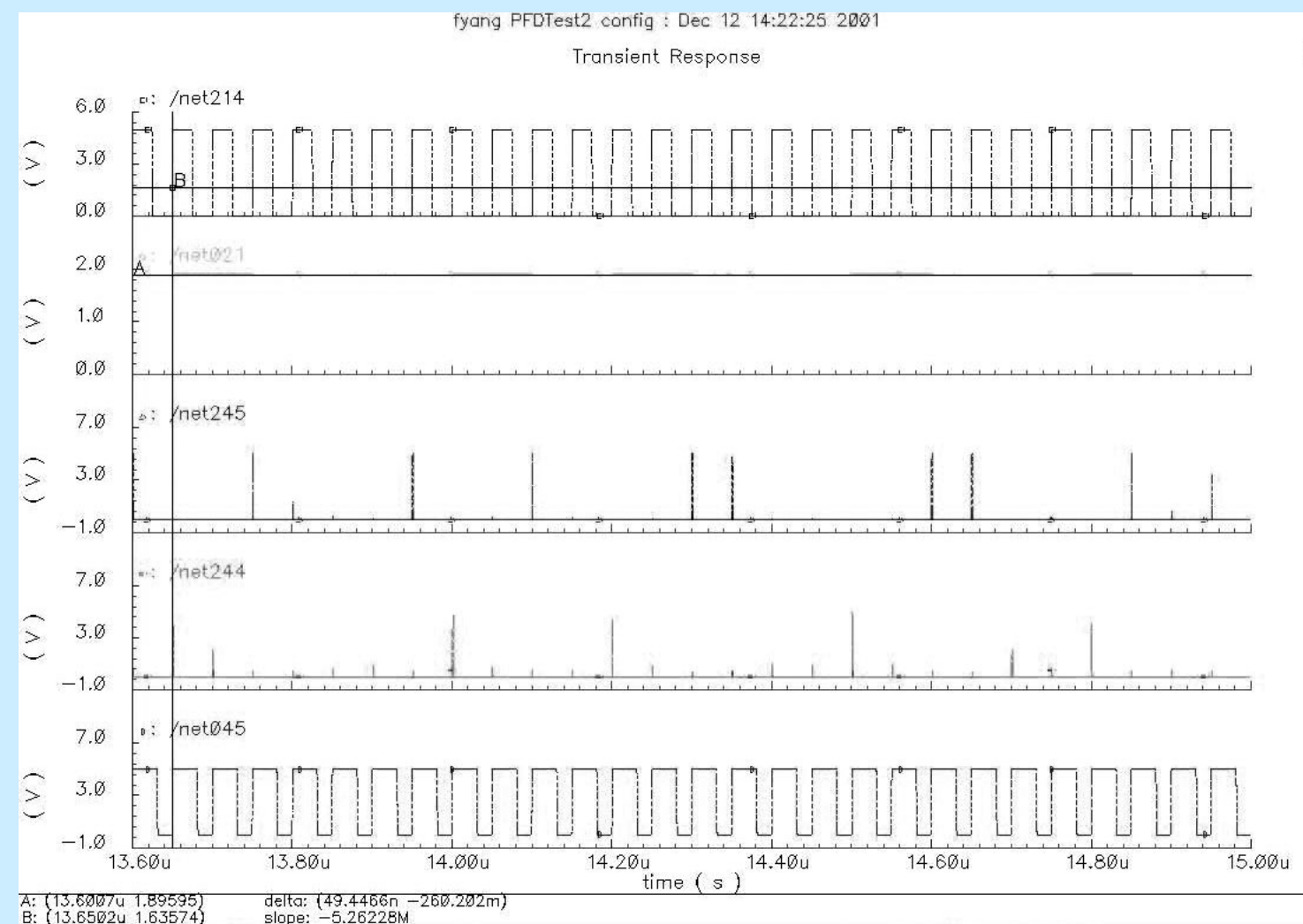


Figure 8. Waveforms of input, outputs of PFD, loop filter and output of PLL (after locking-in)

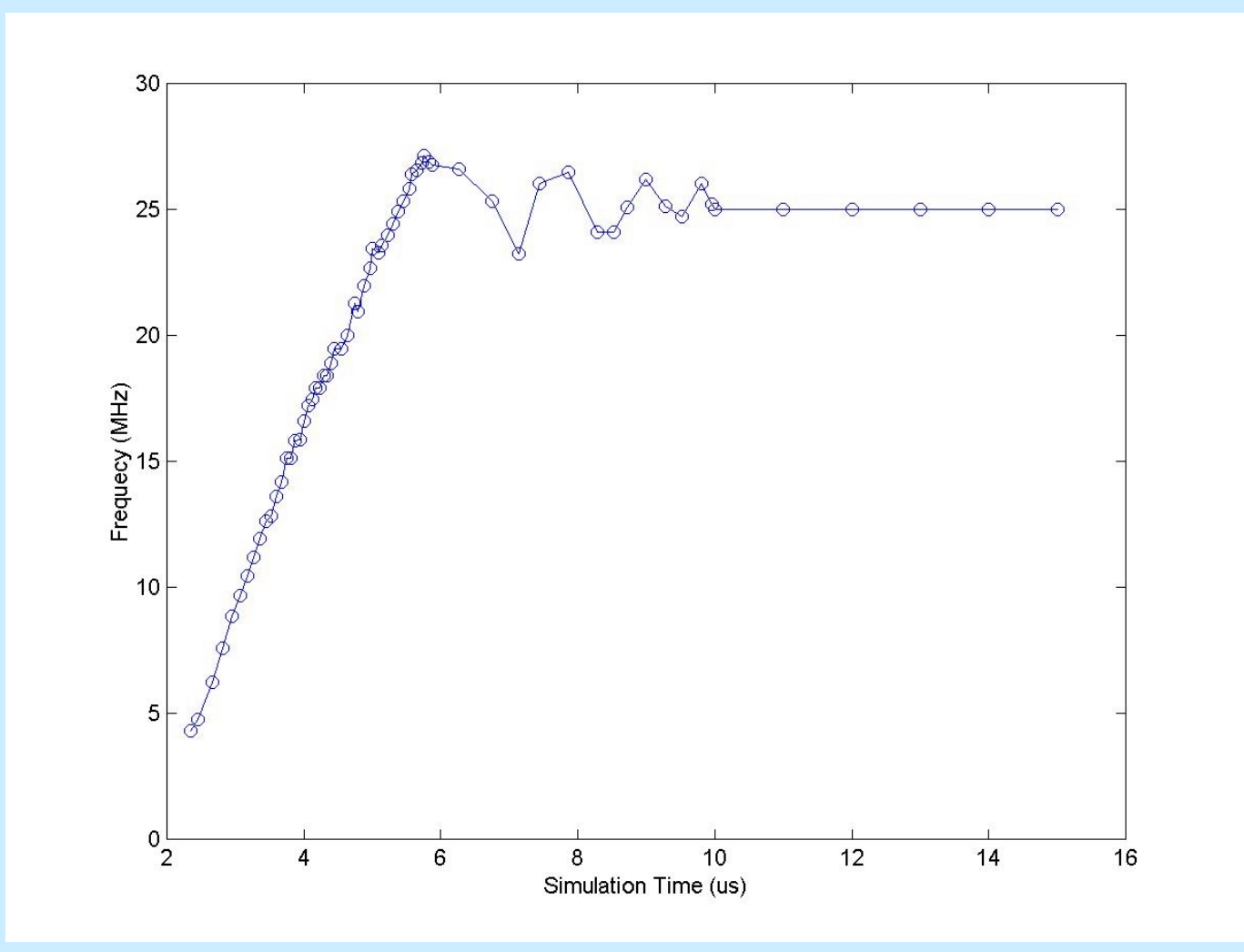


Figure 9. Output frequency of PLL as a function of time

Test

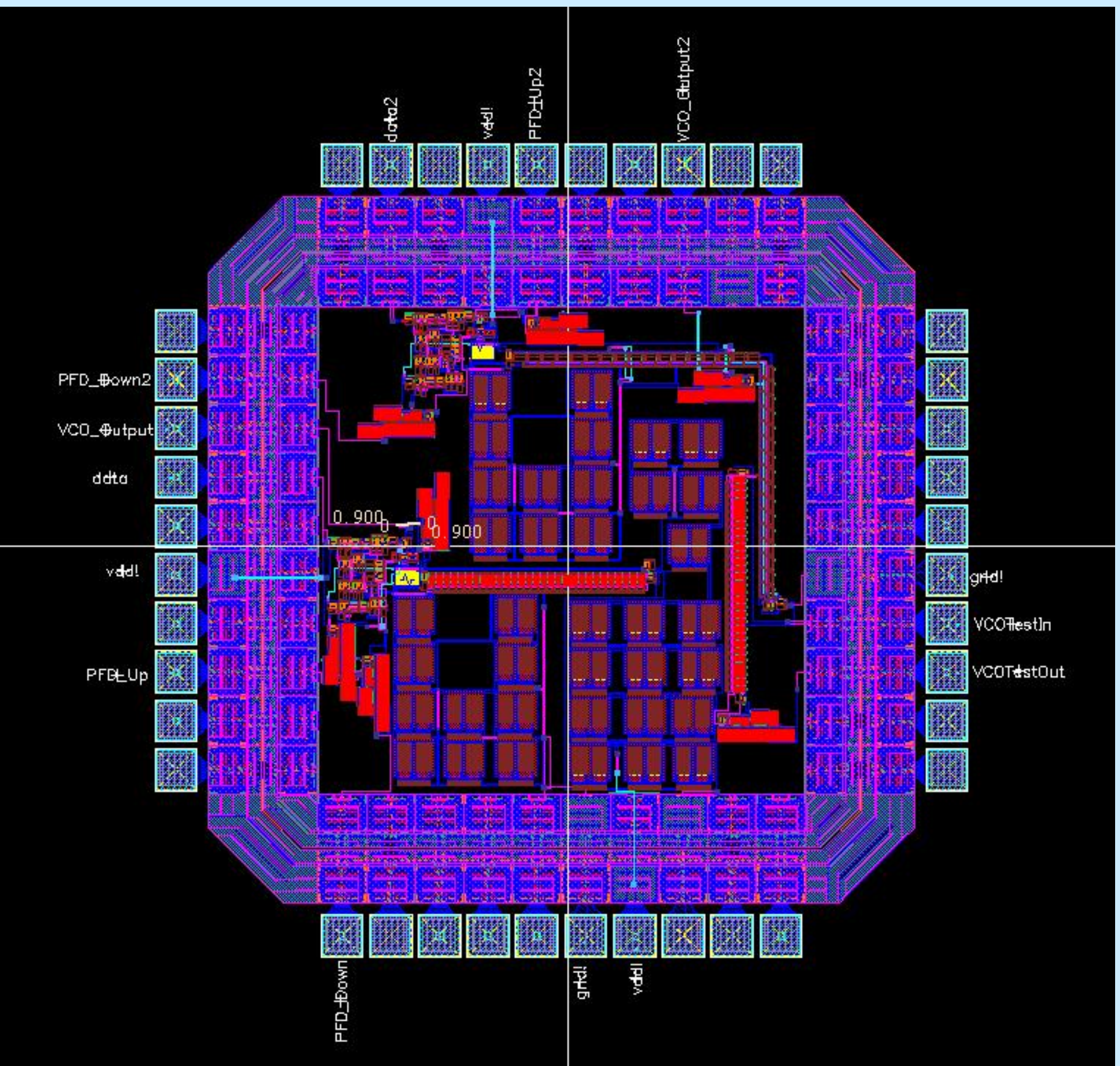


Figure 10. Layout of the whole PLL

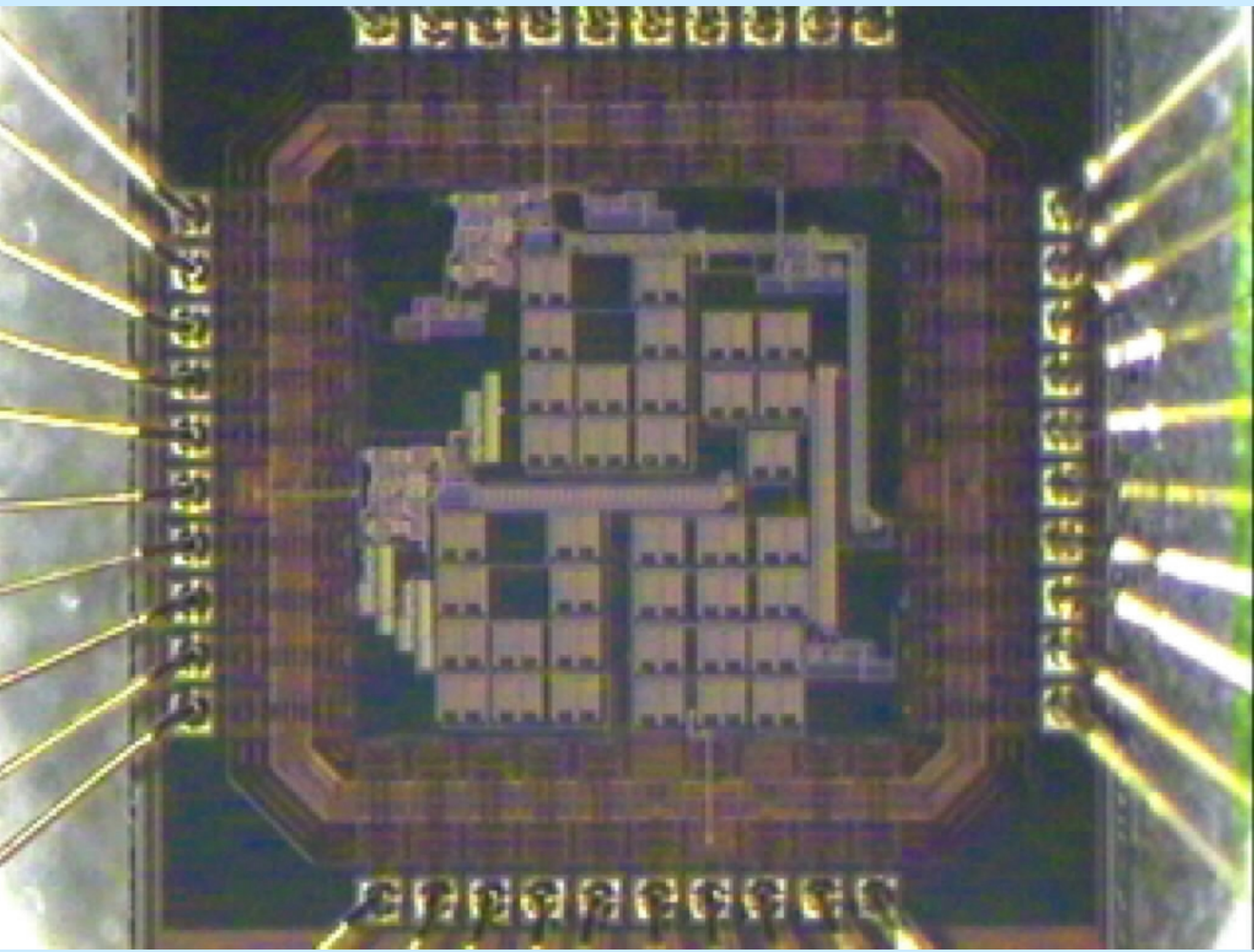


Figure 11. The structure of the actual chip (photo taken via microscope)

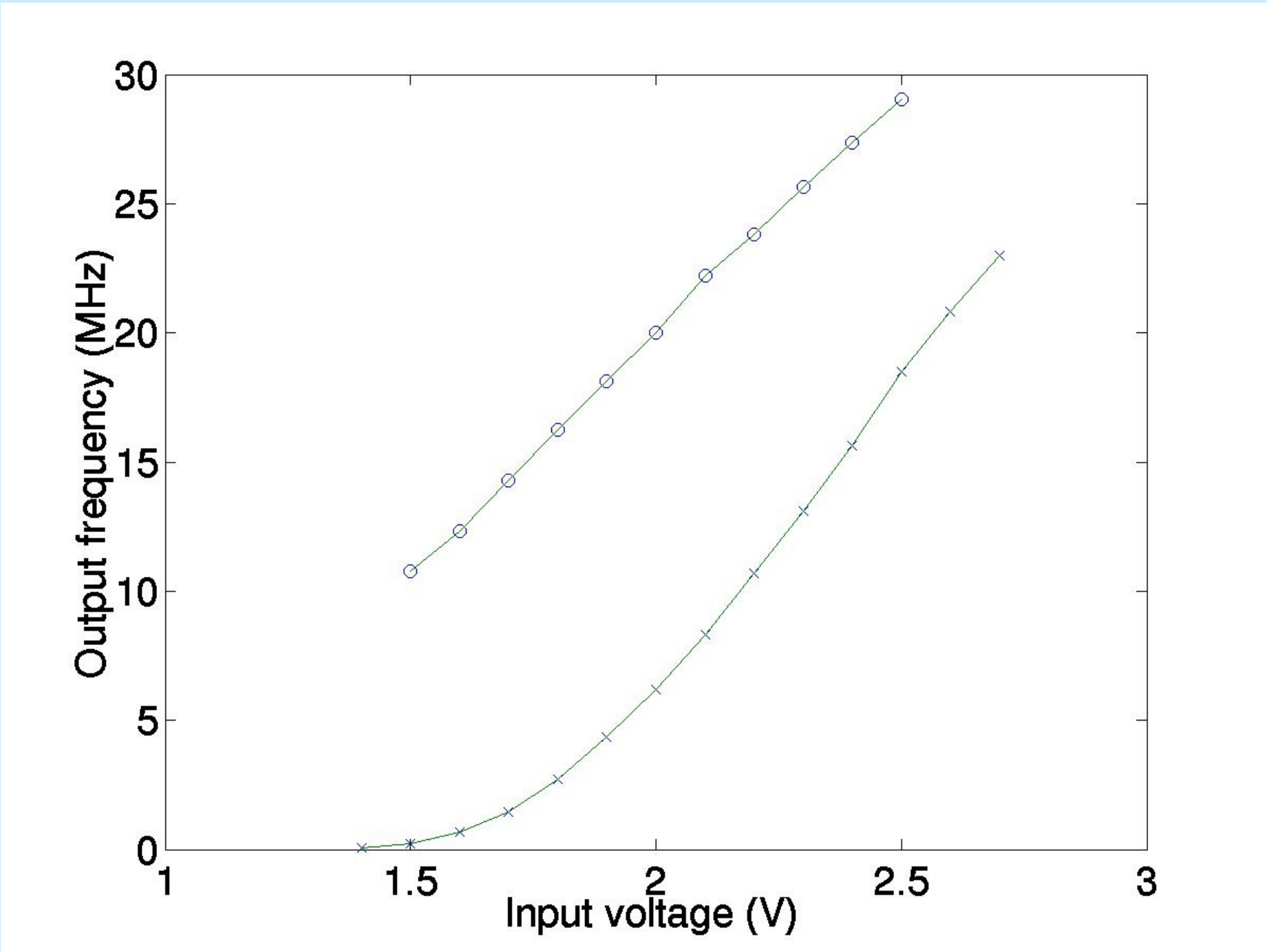


Figure 12. Output frequency of VCO as a function of input voltage

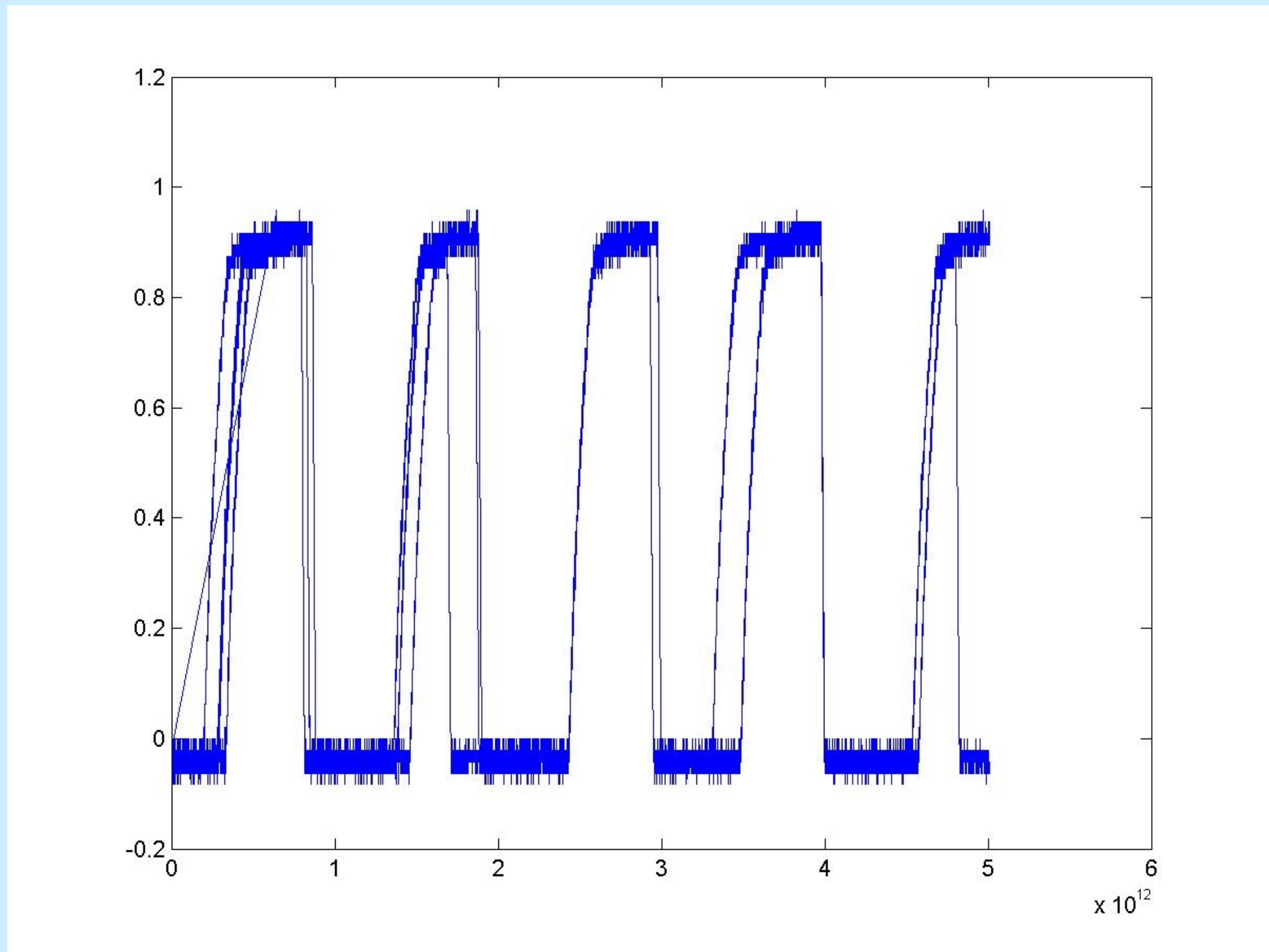


Figure 13. Output waveform of VCO

Comparison between test and simulation:

- The actual output signal of VCO is not the ideal square wave.
- The output frequency vs. input voltage function changes. Compared with the simulation result, the VCO needs higher voltage to generate the same frequency.

Conclusion:

- The simulation results are good.
- The circuit works. But the test results are not ideal. The test data are a little different from the simulation data.