6.Experimental Results

6.1.Static Power

Figure 1 and 2 show the current vs. voltage curves of the two sets of PLL. The voltage range is between 1 and 6 volts.

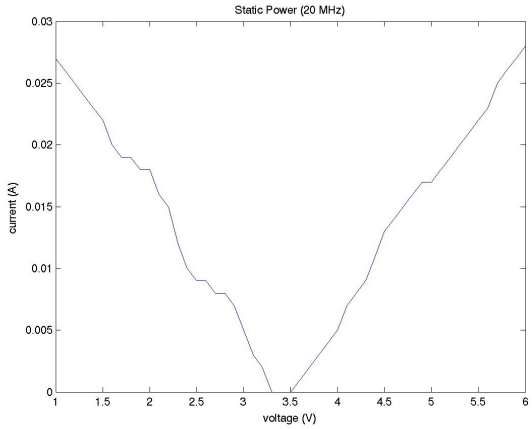

Figure 6.1 Static Power of 20 MHz PLL

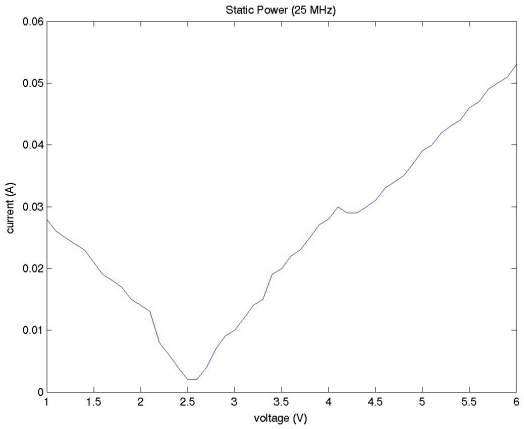

Figure 6.2 Static Power of 25 MHz PLL

6.2.Voltage Controlled Oscillator (20 MHz)

The test data of VCO are different from the results of simulation – the waveform ,amplitude of output signal and the frequency vs. input voltage function.

6.2.1 Waveform

The output waveform is not as good as the simulation one. The actual waveform is not good square wave, especially at high frequency. Figure 6.3 and 6.4 show the waveforms of below 1Hz and 20M Hz (The input voltages are about 1.2V and 2.6V respectively).

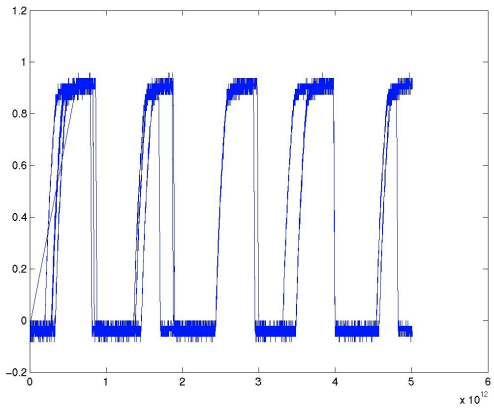

Figure 6.3 Output waveform of VCO (<1M Hz)

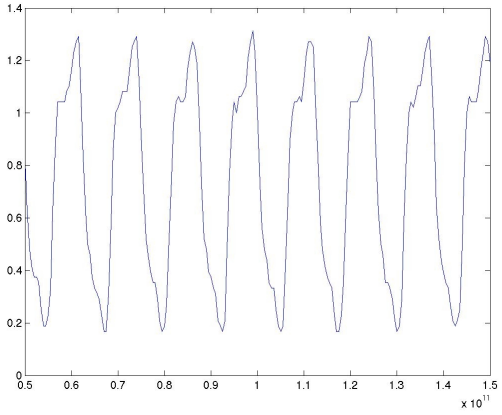

Figure 6.4 Output waveform of VCO (20M Hz)

6.2.2 Output frequency vs. Input voltage

The output frequency vs. input voltage function changes, too.

Compared with the simulation result, the VCO needs higher voltage to generate the same frequency.

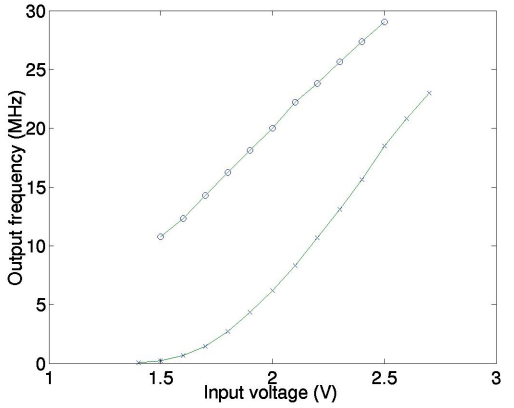

Figure 6.5 Output frequency of VCO as a function of input voltage

Figure 6.5 shows the output frequency of VCO as a function of input voltage for both simulation data and test data under room temperature (about 20 ^{o}C). In the figure, 'o's show the simulation data and 'x's show the test data. We can see from Figure 6.5 that the VCO needs an input voltage of 2.6V to get an output of 20 MHz instead of 2.0V in simulation.

6.2.3 Output amplitude vs. frequency

The amplitude of the output signal is not a constant around 5 volts as the simulation result shows, but decreases with the increase of output frequency (which changes with input control voltage). Figure 6.6 shows the curve of output amplitude vs. output frequency.

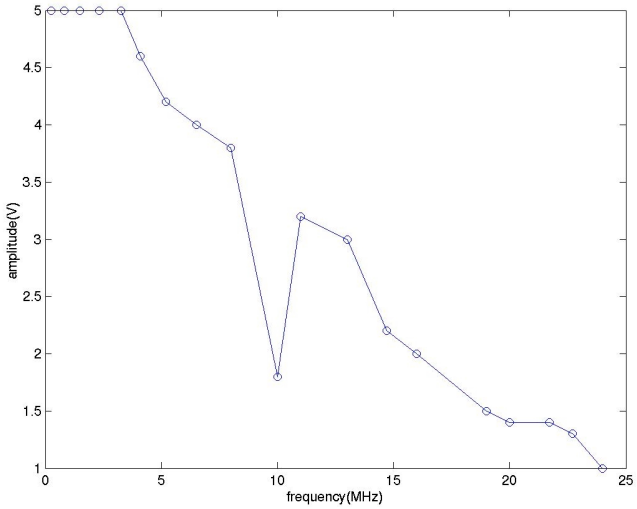

Figure 6.6 Output amplitude of VCO as a function of output frequency

6.3 Temperature effect

The output frequency vs. input voltage function of VCO changes with temperature. But the temperature effect has

not been tested successfully because of the condition of devices and my inexperience. What appeared on the oscilloscope is not a stable waveform, so I can't test the frequency of the signal.

6.4.Phase & Frequency Detector

Because the waveforms of PLL and input data are not square waves and they are different from each other, the PFD always has some outputs, and the outputs are not good square pulses as shown in simulation. But after locking-in, the amplitudes of the UP and DOWN outputs of PFD are small except for the pulses.
Figure 6.7 and 6.8 show the outputs of the PFD.

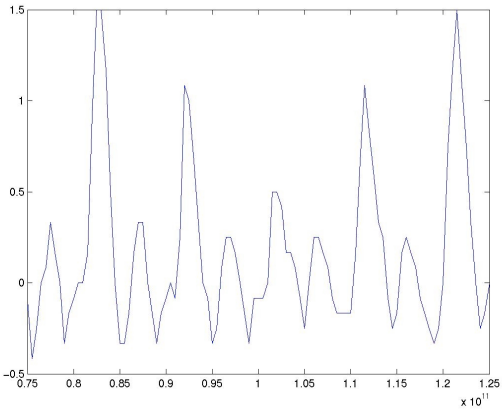

Figure 6.7 PFD UP output signal

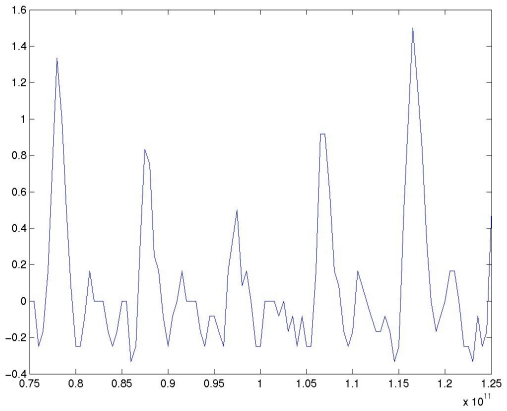

Figure 6.8 PFD DOWN output signal

6.5.Phase-Locked Loop (20 MHz)

The frequency of output signal of PLL can follow the frequency of input data. But the output waveform is far from s quare wave. The reason of this result may be that both the input signal and the output signal of the VCO are not good square wave and the outputs of PFD are not good pulses and are not zero even after locking-in.
Figure 6.9 shows the output signal of PLL.

The locking-in range is [11MHz, 30MHz]. That is, the output frequency of PLL can catch up with the input frequency if the frequency of the input signal is between 11MHz and 30MHz.

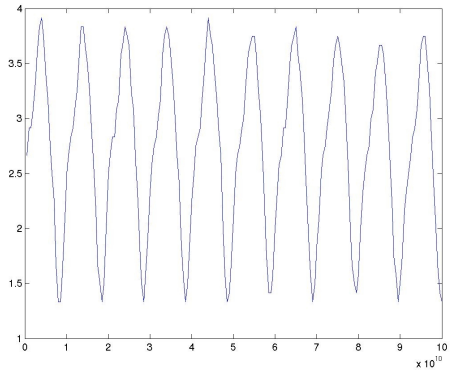

Figure 6.9 Output signal of PLL (20 MHz)

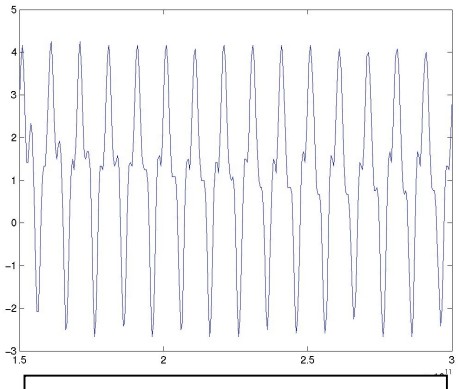

Figure 6.10 Output signal of PLL (25 MHz)

6.6.Phase-Locked Loop (25 MHz)

The condition of this PLL is similar to what is presented in 6.5, and the waveform is even worse.

Figure 6.10 shows the output signal.

The locking-in range of this PLL is [19MHz, 31MHz]. That is, the output frequency of PLL can catch up with the input frequency if the frequency of the input signal is between 19MHz and 31MHz.

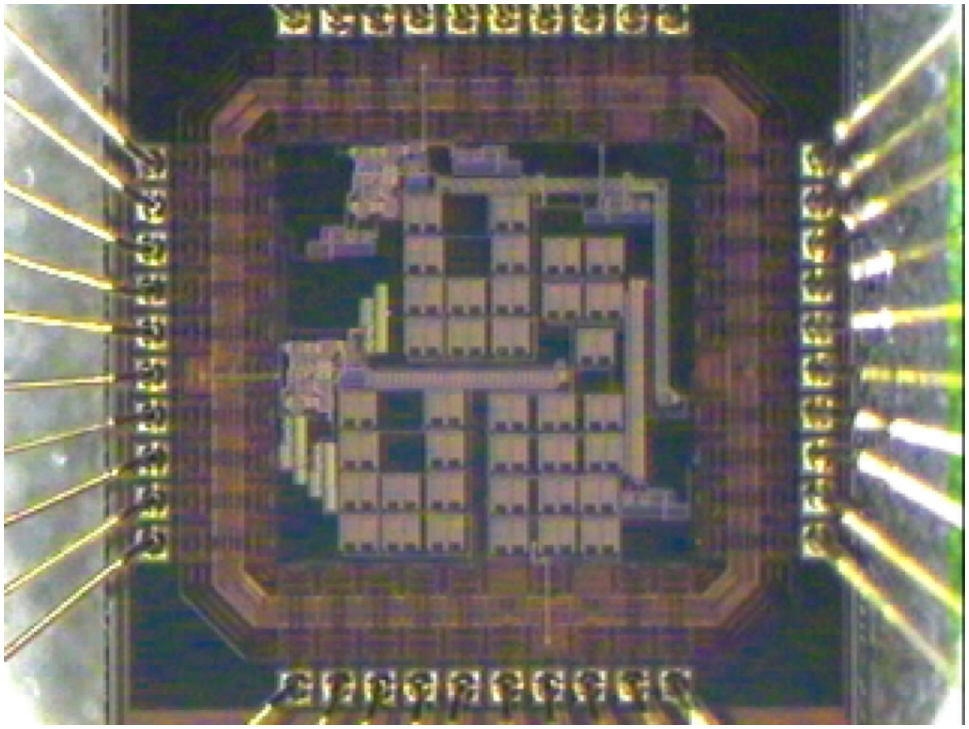

Figure 6.11 Structure of the actual chip