1 Introduction

1.1 **Project overview**

Our Project in ECE547--VLSI Design and Layout is to design a high-frequency digital phaselocked loop (PLL). We propose to implement two different frequencies: one is 20 MHz, another one is 25 MHz.

Usually, a PLL circuit is used to synchronize an output signal, which is usually generated by an oscillator, with a reference or input signal in frequency as well as in phase. In the synchronized state, the difference (error) between the reference and the oscillator output is zero or at least very small. So it is called 'locked'.

The whole circuit consists of three main parts. They are phase & frequency detector (PFD), loop filter (LP) and voltage control oscillator (VCO). The diagram of the PLL is shown in Figure 1.1.



Figure 1.1. Project's diagram

 f_i

fo

- \swarrow The input (or reference) signal: $U_i(t)$
- \swarrow The frequency of the U_i(t):
- \swarrow The output signal of the VCO: $U_o(t)$
- \swarrow The frequency of the U_o(t):
- \ll The output signal of the Loop filter: $U_{f}(t)$

According to the block diagram above, we can clearly explain how this PLL circuit works.

First, we assume that the frequency of the input signal f_i and the frequency of the output f_o are the same. That means there is no phase error in this PLL. So the output of phase and frequency detector $U_d(t)$ must be zero. Therefore, the output signal of loop filter should be a constant value. This constant voltage is to be used as the input to the voltage controlled oscillator. Constant input voltage to the VCO will result in constant frequency of the output signal of that VCO. Thus, the output frequency of $U_o(t)$ is stable locked at the value of f_o , which is equal to the input frequency f_i . This is the condition that permits the VCO to operate at its center frequency. The circuit is locked!

If the phase error is not zero initially, the PFD would develop a nonzero output signal $U_d(t)$, which represents somehow the phase difference between the input signal and output signal of VCO. So the output of the loop filter $U_f(t)$ will not be a constant value. It changes on a basis of the output of PFD. Because different input voltage as input to VCO will change output frequency of VCO to make that output frequency become closer to the reference. After some time, when the output frequency of VCO becomes the same as the input frequency (signal). As described above, in this situation, we call the circuit is stable and locked!

1.2 Objective of project

The first PLL ICs appeared around 1965 and were purely analog devices. An analog multiplier (four-quadrant multiplier) was used as the phase detector, the loop filter was built from a passive or active RC filter, and the well-known voltage controlled oscillator (VCO) was used to generated the output signal of the PLL. This type of PLL is referred to as the "linear PLL"(LPLL) today.

The first digital PLL(DPLL) which appeared around 1970, however, it contained both digital and analog parts. After a few years, the "all-digital" PLL was invented. The ADPLL is exclusive built from a digital blocks, hence doesn't contain any passive components like resistors and capacitors. The last type of the PLL is the SPLL---"software PLL". PLLs can also be implemented by software. In this case, the function of PLL is performed by software.

In a conclusion, there are four types of PLL: The LPLL(linear The DPLL(digital PLL) The ADPLL(all-digital PLL) The SPLL(software PLL)

PLL)

In our project, we propose to implement a high frequency DPLL Our objective is to design a PLL for high frequency signal whose frequency is at least as high as 20 MHz. As we know, last year, one group also dealt with PLL. However, they design their PLL circuit suitable for 10 MHz input signal. That is also high frequency PLL, but it is not high enough. We try to double that frequency to make them even larger. Our PLL is to design for being used in some specific circuit design, such as Carrier-Recovery, Data synchronization, demodulator, and so on.

1.3 Table listing of specifications

1.3.1 The design specification

| Name | Specification |
|--|-------------------|
| The frequency of input signal to PFD | 20 MHz and 25 MHz |
| The voltage of input signal to PFD | 5V |
| The center voltage of VCO | 2V |
| The corresponding frequency of the output of | 20 MHz and 25 MHz |
| VCO when the input voltage to the VCO is | |
| the center voltage of VCO | |
| VSS | GND! |
| VDD | 5V |

 Table 1.3.1
 Design specification of PLL

1.3.2 The test specification:

Test specification of DPLL:

| Name | Specification |
|--------------------------------|-----------------|
| The input Voltage to PLL | 5V |
| The reference frequency of PLL | 20MHz and 25MHz |
| Testing Time | 15 us |

 Table 1.3.2
 Test specification of DPLL

Test specification of PFD:

| Name | Specification |
|--------------------------|---------------|
| The input Voltage to PLL | 5V |

| Data: the reference input | 20MHz |
|---|--|
| Data1: the other input which is consider as the feedback from VCO | 20 MHz, but has Phase difference 25 MHz |

 Table 1.3.3
 Test specification of PFD

Test specification of VCO:

| Name | Specification |
|-----------------------------|---------------|
| The Voltage of input to VCO | 1.5V~2.5V |

| Table 1.3.4 Te | est specification | of VCO |
|----------------|-------------------|--------|
|----------------|-------------------|--------|

1.4 Table of Macros

| Name | Description | |
|------------------------------------|---|--|
| Phase and frequency detector(PFD) | PFD detector is used to find the phase difference and frequency difference between the input signal and the feedback signal from the output of voltage controlled oscillator | |
| Loop Filter(LF) | Connect PFD to VCO. | |
| Voltage controlled oscillator(VCO) | VCO is used to output different Frequency according to different input voltage. | |

Table 1.4.1The Macros of PLL

| Name | Number |
|-------------------|--------|
| 2 input NAND gate | |
| 3 input NAND gate | 2 |
| 4 input NAND gate | 1 |
| Inverter | |

Table 1.4.2The components of PFD

| Name | Components |
|----------------|---------------------|
| Charge pump | 2 PMOS, 2 NMOS |
| Filter | Resistor, Capacitor |
| TE 11 1 1 0 TE | |

Table 1.4.3The components of LF

| Name | Number |
|-----------|----------|
| DelayCell | 29 or 33 |
| Inverter | |

| Table 1.4.4 | The components | of VCO |
|--------------------|----------------|--------|
|--------------------|----------------|--------|

| Pin | Pout | Pinout |
|-----------|-------------|--------|
| data | VCO_Output | gnd! |
| data1 | VCO_Output2 | vdd! |
| VCOTestIn | VCOTestOut | |
| | PFD_Down | |
| | PFD_Down2 | |
| | PFD_Up2 | |
| | PFD_Up2 | |

1.5 Table of PinOuts

| Tables. The name of the This we used | Table5. | The name | of the | Pins | we ı | used |
|--------------------------------------|---------|----------|--------|------|------|------|
|--------------------------------------|---------|----------|--------|------|------|------|

All the information regarding to which pin we choose to use is shown in Appendix C.

1.6 Known limitation of current design

One of the limitations of current design is that simulating the whole circuit would be very time-consuming. Another limitation is that the output signal of VCO has some difference between the width of signal "low "and signal "high". Detailed explanation is in the part 2.2 --- Discussion of design tradeoffs.

2 Circuit Design

2.1 Component description

2.1.1 Phase and frequency detector

The first component in our DPLL is the phase and frequency detector. The output of the PFD depends on both the phase and frequency of the inputs. This type of phase detector is also

termed a sequential phase detector. It compares the leading edges of data and data1 (data is the input signal to PFD, data1 is considered as the feedback signal from the output of VCO to PFD). A data1 rising edge can not be present without a data rising edge. If the rising edge of the data leads the data1 rising edge, the "Up" output of the phase detector goes high while the "Down" output remains low. This causes the data1 frequency to increase and makes the edges move closer. If the data1 signal leads the data, "Up" remains low while the "Down" goes high. And we can find the phase difference between data1 and data.

There are several characteristic of PFD which can be described as below:

- A rising edge from the data and data1 must be present when doing a phase comparison.
- \swarrow The width of the data1 and the data is irrelevant.
- Solution The output of the "Up" and "Down" of the PFD are both low when the circuit is locked. It will cause the output of the filter a constant value

2.1.2 Loop filter

The second component in our DPLL is the loop filter. In our circuit, the loop filter consists of two parts: the charge pump and the RC-filter.

The output of the PFD should be combined into a single output to drive the loop filter. In our project, we use the charge pump to implement it. In charge pump, two NMOS and two PMOS are connected serially. The uppermost PMOS and lowermost NMOS are considered as the current source and the other PMOS and NMOS in the middle are connected to the "Up" and "Down" of the output of PFD, respectively (Be careful that the PMOS in the middle is not connected with "Up" directly. There is an inverter between them). When the PFD "Up" signal goes high, the PMOS will turn on (because that the signal from the inverter goes low). This will connect the current source to the loop filter. It is in the similar way when the PFD "Down" signal goes high.

The loop filter is a simple RC filter, However, it plays a very important role in the DPLL. Unless the loop filter values are correctly chosen, it would take the loop too long to lock or once locked it is still "unstable" -- small variations in the input data may cause the loop unlock again.

If the rising edge of data leads that of data11, the PFD "Up" goes high. And it will cause the voltage of the output signal of the loop filter become higher. If the rising edge of data lags that of data1, the PFD "Down" goes high. It would cause output signal of the loop filter become lower.

2.1.3 Voltage controlled oscillator

In the VCO, the main part is the multiple stage oscillator which is similar to the ring oscillator. In each stage, there are two PMOS and two NMOS. The uppermost PMOS and lowermost NMOS operate as current source and the PMOS and NMOS in the middle operate as inverter. The current sources limit the current available to the inverter. Compared with the resistance and capacitance present in the loop filter, the resistance of the VCO should be

designed infinite and the capacitance of the VCO should be designed smaller.

The input to the VCO is the output signal of loop filter. When the voltage of the input signal to VCO is high, the frequency of output signal in VCO becomes larger and larger. On the contrary, when the voltage of the input signal to VCO is low, the frequency of output signal in VCO becomes smaller and smaller. This is reasonable. For example, if the voltage of the input signal to VCO becomes high, that means the rising edge of data leads that of data1. That is the reason why we need to make the frequency of the output signal of VCO larger to catch up with the reference (input) signal.

2.2 Discussion of tradeoff

First, when we test the VCO, from the simulation result, we just found that in each period, the width of low and the width of high are different. This will affect the final output from PLL. This means when the PLL is locked, we can still find the difference between the width of low and the width of high in each period of the feedback output. The reason why it is different is that in our design, the ratio of width and length in PMOS and NMOS is too different. If we change the ratio of width and length in PMOS and make it closer to the NMOS, it will improve our result. However, it will make the frequency of the output signal from the VCO very high. We have to add some more stage to keep the frequency lower. From our experiment, if we change the ratio of width and length in PMOS to as twice as that in NMOS, we have to add to at least 61 stages. So there is a trade off here: Keeping the ratio of width and length in PMOS closer to the ratio of width and length in NMOS will result in that difference between the width of low-to-high and the width of high-to-low in the waveform of VCO result similar to each other. However, it will cause the output frequency very high. We have to add a lot of stages to make it lower. So I have to find a balance point between these two to find a best one.

Second, in the RC filter, if we choose a very small capacitor, the charge pump would charge and discharge the capacitor very quickly. It would cause the voltage of the output of loop filter to go up also very quickly. This would make the output signal of the VCO oscillate very frequently and thus can not be locked. To solve this problem, we have to increase the value of that capacitance. Although it would increase the time for simulation and make the test process time-consuming, the PLL at last can be locked.

2.3 Description of schematics

2.3.1 Phase and frequency detector schematics

The phase and frequency detector is composed of six 2-input NAND gates, two 3-input NAND gates, one 4-input NAND gates and eight inverters.

In 2-input NAND, the pull up network consists of 2 PMOS, which are connected parallelly. The pull down network consists of 2 NMOS, which are connected serially. The sizes of the two PMOS are the same as the size the two NMOS. The width of NMOS is 30um and the length of NMOS is 600nm. The width of the PMOS is 30um and the length of NMOS is 600nm. For the 3-input NAND gates and 4-input NAND gates, the pull up networks have 3 or 4 PMOS respectively and they are connected parallelly. And the pull-down networks consist of 3 or 4 NMOS respectively and they are connected serially. All the NMOS and PMOS have the same size as those in 2-NAND gates. In all NAND gates, the pull-up networks are connected to VDD, which is 5V and the pull down networks are connected to GND.

The PFD has two input pins and two output pins. One of the input pins is connected to the input (reference) signal. The other one is connected to the feedback signal from the output of VCO. The two output pins are called "Down" pin and "Up" pin respectively, and they are connected to the charge pump as the inputs to the charge pump loop filter.

If the data leads data1,

2.3.2 Loop filter schematics

The loop filter macro is composed of two main parts. One is the charge pump and the other one is the RC-filter.

Charge pump consists of two PMOS and two NMOS, which are connected serially. Both of the NMOS are in the pull down section and both of the PMOS are in the pull up section. The gate of uppermost PMOS is connected to GND. The gate of lowermost NMOS is connected to VDD. The gates of the remaining NMOS and PMOS are connected to the "Down" pin and "Up" pin of the output of PFD. The width of the uppermost PMOS is 15 um and the length of it is 7.5 um. The width of the other PMOS is 30 um and length of it is 600 nm. The width of the lowermost NMOS is 7.5 um and length of it is also 7.5 um. The width of the other NMOS is 15 um and the length of it is 600 nm.

The RC filter consists of 2 resistors and 1 capacitors. The resistor, which is directly connected to the output of charge pump, has the resistance of 500 kOhm. The other one which is connected with capacitors has the resistance of 2 kOhm. The capacitance of the capacitor is 20 pF.

2.3.3 Voltage controlled oscillator

The main part of the voltage controlled oscillator is the multiple stage oscillator. Each stage is called DelayCell. In the DelayCell, there are two PMOSs and two NMOSs, which are connected serially. Each DelayCell has three inputs A, BVC and one output. Each A is connected together. Each Vc is connected together! Each B is connected to next stage's output. The width of the two PMOSs is 22.5 um and the length of them is 600 nm. The width

of the two NMOSs is 1.8 um and the length of them is 600 nm. The Vdd is connected to the uppermost PMOS. The gnd is connected to the lowermost NMOS.

3 Circuit Performance

3.1. Schematic simulation results

3.1.1. Results for some important components (other than macros)

NAND



Charge Pump:

Result 1:

The figures 3.2 shows the simulation results for PFD and charge pump together. Two pulse voltage sources are used as the input signals of the Phase and frequency detector. One is

treated as the input of the whole PLL, and the other is treated as the feedback from VCO. The two signals have the same frequency and different phases. The output of the PFD is the input signal of the charge pump. Figure 3.2 shows the waveforms when the phase of feedback from VCO leads that of the input signal. The Down pin of the PFD outputs the phase difference between the two inputs of PFD. Then the charge pump discharges the capacitor of the loop filter. The voltage of the capacitor becomes lower and lower. This voltage is the control voltage of VCO. Thus, the output frequency will become lower. Its frequency and phase will change to match the input signal.



Figure 3.2 Simulation result (1) for Charge Pump

Result 2:

Figure 3.3 shows the waveforms when the phase of feedback from VCO lags that of the input signal. The Up pin of the PFD outputs the phase difference between the two inputs of PFD. Then the charge pump charges the capacitor of the loop filter. The voltage of the capacitor becomes higher and higher. Thus, the output frequency will become higher. Its frequency and phase will change to match the input signal.



Figure 3.3 Simulation result (2) for Charge Pump

3.1.2. Results for large macros

3.1.2.1 Phase and frequency detector:

Result 1: Transient Response I for PFD

The test circuit is similar to that to test the charge pump. Figure 3.4 shows the waveforms when the phase of feedback from VCO leads that of the input signal. Net3 is input signal to the PLL, net5 is the feedback from VCO. Net14 is the Down output of PFD.



Figure 3.4 Simulation result (1) for PFD

Result 2: Transient Response 2 for PFD

Figure 3.5 shows the waveforms when the phase of feedback from VCO lags that of the input signal. Net 10 is the Up output of PFD.



Figure 3.5 Simulation result (2) for PFD

Result 3: Transient Response 2 for PFD

Figure 3.6 shows when the two inputs of the PFD have different frequencies. One is 20MHz, and the other is 25 MHz. In a time period of 200ns, one has four periods and the other has five periods. We can see from the figure that the output pulse width becomes larger and larger because the phase difference increases. But at the time of 200ns, the two signals have the same phase. So the output is 0.



Figure 3.6 Simulation result (3) for PFD

3.1.2.2 Voltage controlled oscillator

Result 1: DC Simulation (For 20MHz VCO)



Figure 3.7 DC Simulation result for VCO (20MHz)

The figure shown above is the frequency vs. control voltage of 20MHzVCO. The X coordinate is the control voltage of VCO and the Y coordinate is the frequency of the output signal. It is perfect linear for an input voltage range between 1.5V and 2.5V with the output frequency between 11MHz and 29MHz. Its central point is at 2V, the corresponding output frequency is 20 MHz.

| Control voltage | Period of output signal (ns) | Frequency of output signal (MHz) |
|-----------------|------------------------------|----------------------------------|
| 1.5 | 93 | 10.75 |
| 1.6 | 81 | 12.34 |
| 1.7 | 70 | 14.28 |
| 1.8 | 61.5 | 16.26 |
| 1.9 | 55.2 | 18.11 |
| 2.0 | 50 | 20 |
| 2.1 | 45.46 | 22.22 |
| 2.2 | 42 | 23.80 |
| 2.3 | 39 | 25.64 |
| 2.4 | 36.53 | 27.37 |
| 2.5 | 34.43 | 29.04 |

Result 2: DC Simulation (For 25MHz VCO)

The figure shown below is the frequency vs. control voltage of 25MHz VCO. It is similar to the Figure 3.8. The X coordinate is the control voltage of VCO and the Y coordinate is the frequency of the output signal. It is linear for an input voltage between about 1.5V and 3V with the output frequency between 11MHz and 29MHz. Its central point is at 2V, the corresponding output frequency is 25 MHz. This VCO is not as good as that of 20MHz. But it has a wider linear range.



Figure 3.8 DC Simulation result for VCO (25MHz)

Result 3: Transient Response (For 25MHz VCO)

The figure 3.9 is the transient response of the VCO. We can see clearly from the figure that the output frequency changes with the input voltage linearly. But the pulse width of the output of VCO is not 50%. This is determined by the different sizes of the PMOS and NMOS used in the delay cell and thus the high to low process and low to high process need different time. It will cause a problem, which will be discussed later.



Figure 3.9 Transient Simulation result of VCO

3.1.2.3 Loop Filter

Result : Transient Response (see figure 3.10)



Figure 3.10 Simulation result for PFD

3.1.3 Entire circuit

Result 1. Transient Result for PLL (20 MHz)

The figure 3.11 is the simulation result for the whole 20MHz PLL. Net214 is the input to the PLL; net045 is the output of PLL; net023 is the output of the loop filter as well as the input control voltage of the VCO; net245 is the Down output of the PFD and net 244 is the Up output of the PFD. The simulation time is 15 us.

At first, when the control voltage is not high enough, the VCO doesn't oscillate. It begins to oscillate at the voltage of about 1.5V. The output frequency is lower than the input frequency, so the Up output of PFD has pulses and the output of loop filter continues to increase. At a point, the output phase leads the input phase. Then the Down output begins to have pulses. The Up and Down outputs have pulses alternatively until the phase and frequency of the input and output are almost the same, that is, the PLL has locked in. The output of the filter remains at about 2V.

The locking-in time is about 10 us. But we can see there are some pulses of the Up and Down outputs after 10 us. The reason of this phenomenon has been mentioned before. The pulsed width of the output signal is not 50%, but the input signal is a symmetric square wave. So there are some phase difference even after locking-in.



Figure 3.11 Transient Result for PLL (20 MHz)

Result 2. The transient response result for PLL which is in the stable section (20MHz)

The figure shown 3.12 is the last part of the previous figure. It's in the locking in section. The output of the loop filter doesn't change. It remains at about 2V. The phase and frequency of the VCO output is the same as the input of the PLL. We can see clearly here that the output signal is asymmetric.



Figure 3.12 The transient response result for PLL which is in the stable section (20MHz)

Result 3: Transient Result for PLL (25 MHz)

The figure 3.13 is the simulation result for the whole 25MHz PLL. It is similar to that of the 20MHz PLL. The locking-in time is also about 10 us.



fyong FFDTest2 config : Dec 14 15:11:17 2001

Figure 3.13 Transient Result for PLL (20 MHz)

Result 4: The transient response result for PLL which is in the stable section (25MHz)

The figure 3.14 is the last part of the previous figure. It is similar to that of the 20MHz PLL. It has the same problem about the pulse width.



Figure 3.14 The transient response result for PLL which is in the stable section (25MHz)

3.2 Discussion of results

Based on a lot of experiments, we find that our PLL works well. Figure 3.15 basically shows how the circuit works (This is also a testing for PLL 25 MHz). The X axis is the simulation time. The Y axis is the output frequency at the corresponding time. In this figure, we can find that there are four sections. The first section is before nearly 2.3 us. In this section, we can not observe if the output signal oscillate or not. The output voltage from loop filter is very low, so either the output signal does not oscillate or it oscillates with very low frequency, which can not be observed in a short time section. The second one is between 2.3 um and 6 um. During this simulation time, we find that the output of VCO becomes oscillating and its frequency becomes higher and higher. That means the output signal wants to catch up with the input reference. The third section is between 6 um and 10 um. At the simulation time 6 um, the frequency of the output signal is higher than that of the input reference, which is 25 MHz. So after that, the frequency of the output begins to decrease until it is lower than 25 MHz, and then it will increase again. We observe that the frequency of output oscillate around 25 MHz and it becomes closer and closer to 25 MHz. The fourth section is after 10 um. In



this section, the figure becomes stable. The frequency of output from VCO reaches 25 MHz and does not change any more. At this time, the PLL is locked.

However, we still have some problems. One of them is the time-consuming issue. Anther problem is about non-equivalent width of output signal. We discuss it in the chapter 2. And this is what needs to be improved.

4 Physical Design

4.1 Description of components

As we have described before, the Phase – Locked Loop has three major parts – phase & frequency detector (PFD), loop filter (LF) and voltage – controlled oscillator (VCO). But there's another important part for the final design – digital buffer. The pins of the chip have high capacitances. If the output signal drives such a capacitance without a buffer, the waveform of the signal will not be what we expected because of the time for charging this capacitor.

The layout of these parts will be described in detail later.

4.2 Layout considerations

For high frequency signals, the waveforms will change when they pass small transistors. The working frequencies of the two PLL are 20 MHz and 25 MHz respectively, so most of the PMOS and NMOS we use have relatively large width. For example, the transistors we use to build inverter and NAND gates have width of 30µm. To make the layout more compact, multiplier is used. We use multiplier of 5, each with width of 6µm for the 30µm MOS. Then we use poly path to connect all the gates together and use metal1 to connect all the sources together and all the drains together. In this way, the sizes of the circuits are much smaller.

In our layout, especially in the two VCOs, the gates of many PMOS and NMOS need to be connected together. In order not to introduce high parasitic resistance of long poly paths, we use metal paths and contacts to connect them.

The considerations will be described in detail when describing the associated physical layout.

4.3 Description of physical layout

4.3.1 Phase & frequency detector

The figure shown in Fig 4.1 is the layout of the whole phase & frequency detector.

The width of the layout is $128.25\mu m$ and the length is $153.75\mu m$. It includes eight inverters, six 2-input NAND gates, two 3-input NAND gates and one 4-input NAND gate. The PMOS and NMOS of all the gates have the same width and length ($30\mu m / 600nm$).



Figure 4.1 Phase & frequency detector

4.3.2 Loop Filter

Loop filter includes charge pump, two resistors (one is 2K Ohm and the other is 500K Ohm) and a 20-pf capacitor. The components of loop filter are shown in figure 4.2 - 4.8.

Charge Pump

The layout of the charge pump is shown below. It includes two PMOS and two NMOS. One

PMOS and one NMOS have a large length of 7.5μ m. They are used as resistors to make the capacitor of the loop filter to be charged slowly so that it's voltage will not change too fast. Then the frequency of the output signal of VCO will change step by step. More metal1-poly contacts are added to connect these large gates.



Figure 4.2 Charge Pump

Resistors



Figure 4.3 2K Ohm resistor



The elec in the highres is 2.55/1.5. The resistance shown in the extracted is 2.026K Ohm. The error is 1.3%. Although it's not exact 2K Ohm, the error is in the allowed range of 10%





Figure 4.5 500K Ohm resistor



The resistance shown in the extracted is 500K exactly.

Capacitor

In layout, a 20-pf capacitor will be very large. So we make ten 2-pf capacitors and connect them together to get the 20-pf capacitor.





Figure 4.8 Extracted of 2-pf capacitor

We can use an elec square of $50.1\mu m$ *50.1 μm to get the 2-pf capacitor. The poly is still too large. There will be high parasitic resistance of such a large poly rectangle. To prevent this, in each capacitor, the elec is separated into two parts which are both 50.1 μm *25.05 μm . More Metal1-poly contacts are added around them.

The capacitance shown in the extracted is 1.001 pf for each part.

4.3.3 Voltage-Controlled Oscillator

There are two Voltage-Controlled Oscillators in our circuit. One has the central frequency of 20MHz and the other of 25MHz.

In VCOs, all the A pins of the delay cells are connected together, so are the Vc pins. The A pin and the Vc pin are connected to the gates of the PMOS and NMOS of the delay cell. To avoid a very long ploy line, Metal2 and Metal3 are used to connect them in the two VCOs respectively.

The layout of the 20 MHz VCO is show in figure 4.9.





The layout of the 25 MHz VCO is similar (refer to Appendix B). But it's much longer than the 20 MHz one. The main reason is that we don't use multiplier in the delay cell for 25 MHz VCO. The width of the PMOS used in the delay cell for 25 MHz VCO is 19.65 μ m, which is 131 times of the grid unit. The multiplier and the number of grid units of each MOS in multiplier must be integer. But 131 is a prime number, so multiplier can't be used for it.

4.3.3 Buffer

A digital buffer is used for every digital output. It's a 4-stage buffer. The first stage has a PMOS of 30μ m and a NMOS of 15μ m. The size of the next stage is 3 times of the previous stage. That is, the second stage has a PMOS of 90μ m and a NMOS of 45μ m; the third stage has a PMOS of 270μ m and a NMOS of 135μ m; the last stage has a PMOS of 810μ m and a NMOS of 405μ m. The buffer is shown in figure 4.10. The first three stages are above the last

stage. We use multiplier for all the PMOS and NMOS in the buffer. All the nwell of the PMOS are connected together with nwell rectangles.



Figure 4.10 Digital Buffer

4.4 Floorplanning issues

Metal3 paths and many M2-M3 contacts are used to connect the outer ring of vdd! pins to allow more current. More M1-Poly, M1-M2 and M2-M3 contacts are used for the same purpose.

We don't use many pins because only an input and an output besides vdd! and gnd! are necessary for a PLL. We add some pins to test the outputs of the Phase & Frequency Detector. A 20MHz VCO is put into the chip to be tested by itself.

Some capacitors are filled in the blank area. These capacitors are just connected between vdd! and gnd!.

Please refer to Appendix B for detailed layout.

5 Verification

5.1 DRC and LVS Verification

All the components of our circuit and the top level design passed the DRC and LVS verification.

There are no errors or warnings of DRC verification, and the net-lists of schematic and extracted match.

The output of top level design LVS verification is listed below.

@(#)\$CDS: LVS version 4.4.5 10/28/1999 15:28 (cds11182) \$

Like matching is enabled. Net swapping is enabled. Using terminal names as correspondence points.

Net-list summary for /usr/grads/fyang/ece547/LVS/layout/netlist

| count | |
|-------|-----------|
| 409 | nets |
| 12 | terminals |
| 4 | res |
| 74 | cap |
| 1416 | pmos |
| 1172 | nmos |
| | |

 $Net-list\ summary\ for\ /usr/grads/fyang/ece547/LVS/schematic/netlist$

| count | |
|-------|-----------|
| 409 | nets |
| 12 | terminals |
| 4 | res |
| 37 | cap |
| 321 | pmos |
| 320 | nmos |
| | |

Terminal correspondence points

- 1 PFD_Down
- 2 PFD_Down2
- 3 PFD_Up
- 4 PFD_Up2

| 5 | VCOTestIn |
|----|-------------|
| 6 | VCOTestOut |
| 7 | VCO_Output |
| 8 | VCO_Output2 |
| 9 | data |
| 10 | data2 |
| 11 | gnd! |
| 12 | vdd! |

The net-lists match.

| | layout | sc | hem | atic |
|---------------|--------|-----|-----|------|
| | instar | nce | s | |
| un-matched | 1 0 | | 0 | |
| rewired | 0 | | 0 | |
| size errors | 0 | | 0 | |
| pruned | 0 | | 0 | |
| active | 2 | 66 | 6 | 682 |
| total | 2 | 66 | 6 | 682 |
| | | | | |
| | nets | | | |
| un-matched | 1 0 | | 0 | |
| merged | 0 | | 0 | |
| pruned | 0 | | 0 | |
| active | 4 | .09 | 409 | |
| total | 4 | .09 | 409 | |
| | | | | |
| | termi | nal | s | |
| un-matched | 1 0 | | 0 | |
| matched bu | t | | | |
| different typ | be 0 | | 0 | |
| total | 1 | 2 | 12 | |

Probe files from /usr/grads/fyang/ece547/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

| termbad.out: |
|--------------|
|--------------|

prunenet.out:

prunedev.out:

audit.out:

Probe files from /usr/grads/fyang/ece547/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

5.2 Simulations of extracted view

For high frequency digital circuits of 20MHz or 25 MHz, the parasitics are not neglectable. But our top-level design works well with extracted parasitics.

The waveforms of simulations of extracted are shown and discussed below. The phase & frequency detector, voltage-controlled oscillator and the whole phase-locked loop are tested separately.



Figure 5.1 Simulation of Phase & Frequency Detector extracted



Figure 5.2 Simulation of Phase & Frequency Detector extracted Cont.

Figure 5.1 and Figure 5.2 show the simulation results of Phase & Frequency Detector extracted. We use a pulse voltage source as the input signal to the whole PLL (data) and use another pulse voltage source as the feedback signal of the VCO (dataclock). These two pulse signals have the same amplitude of 5V and the same frequency but different phases. Figure 5.1 shows the result of simulation when the phase of data leads that of dataclock. The output of the Up pin of the PFD will be pulses whose widths equal to the phase difference between data and dataclock. Figure 2 shows the result of simulation when the phase of data leads that of data leads that of dataclock. The output of the Down pin of the PFD will be pulses whose widths equal to the phase difference between data and dataclock. The output of the same as those of the simulations without parasitics.

But the Voltage-Controlled Oscillators are more sensitive to the parasitics.

The period of the output signal of the 20MHz VCO should be 50ns. But we can see in the Fig4.13 that the period changes to about 45.5ns. That is, the frequency changes to about 21.98MHz. As we have shown before, the linear range of the 20MHz VCO is up to 29MHz. It's still in the linear range. So the PLL can work normally with these parasitics.



Figure 5.3 Simulation of Voltage-Controlled Oscillator extracted (20



Figure 5.4 Simulation of Voltage-Controlled Oscillator extracted (25

We can see from Fig4.14 that the VCO of 25MHz doesn't change much with the parasitics. The period of the output signal is 40.055ns. The change is only 0.125%.

The pulse widths of the two VCO also change a little with the parasitics. The waveforms become more unsymmetric. So with an input signal with square wave, there will be some phase difference all the time even after locking in.

The loop filter is a simple analog RC filter. Including the charge pump, it only has 4 transistors and some resistors and capacitors. It doesn't change at all with paracitics.

6 Experimental Results

Available next semester.

7 Summary and Conclusions

7.1 Comparison between simulation and experimental results

Available next semester.

7.2 Suggestions for improved performance

The output signal of the VCO is not symmetric, that is, the pulse width is not 50%. So there are occasionally some phase differences even after locking in. This problem can be solved by making the PMOS and NMOS of the delay cell have similar widths. But this method will create another problem. We will need much more stages to get the frequency we want.

7.3 Suggestions for improved design

The loop filter we use is somewhat simple. To make the control voltage of VCO change slowly, we have to use a big capacitor of 20 pf. Because of this big capacitor, the lock-in time is a little long (about 10µs). If we design a more complex filter, the lock-in time may be shorter.

The work of design, simulation and layout is challenging and interesting. We learned a lot in this process, not only the knowledge about Cadence, but also the importance of teamwork. We felt excited when the simulation results are the same as what we expected, when our layout pass the DRC verification and especially when the LVS verification output shows "The net-lists match".

We spent several hours every day on this project It's time and energy consuming, but we learned a lot of stuff and got some experience. **We enjoy it!!!**

Acknowledgements

We are grateful for the assistance of Dr. Kotecki and our classmates. Dr. Kotecki helped us solve many problems about design, simulation and layout. We also got much help and stimulation from our classmates.

Appendix A: Schematics

Phase and frequency detector

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Voltage-Controlled Oscillator (20MHz)

Voltage-Controlled Oscillator (25MHz)

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Delay Cell (For 20MHz)



Delay Cell (For 25MHz)



Charge Pump



The whole Phase-Locked Loops



Appendix B: Physical Layout

Phase & frequency detector



Fig B.1 Phase & frequency detector

Loop filter

Charge pump



Fig B.2 Charge Pump

2K Ohm resistor





Fig B.3 2K Ohm resistor

Fig B.4 Extracted of 2K Ohm resistor

500K Ohm resistor



Fig B.5 500K Ohm resistor

Fig B.6 Extracted of 500K Ohm resistor





Fig B.7 2-pf capacitor



Voltage-controlled oscillator (20MHz)



Fig B.9 20MHz VCO

Voltage-controlled oscillator (25MHz)



Fig B.10 25MHz VCO





Fig B.11 20MHz Delay Cell

Fig B.12 25MHz Delay Cell

Phase-Locked Loops (20MHz)



Fig B.13 20MHz PLL

Phase-Locked Loops (25MHz)



Fig B.14 25MHz PLL

Final Design (two sets of PLL)



Fig B.15 Final Design





Fig B.16 Final Chip

Digital Buffer



Fig B.17 Digital Buffer

Appendix C: PinOut Diagram

| Name | Pin Number | C (PF) | description |
|-------------|------------|--------|---|
| Data2 | 34 | 1.48 | Input signal to PLL (25MHz) |
| Vdd! | 32 | 0.863 | 5v |
| PFD_Up2 | 31 | 0.660 | Output of PFD "Up" (25MHz) |
| VCO_output2 | 28 | 1.05 | Output of VCO (25MHz) |
| PFD_Down2 | 37 | 2.34 | Output of PFD "Down" (25MHz) |
| VCO_Output | 38 | 3.37 | Output of VCO (20MHz) |
| Data | 39 | 4.39 | Input signal to PLL (20MHz) |
| Vdd! | 1 | 5.32 | 5v |
| PFD_Up | 3 | 3.37 | Output of PFD "Up" (20MHz) |
| PFD_Down | 6 | 1.43 | Output of PFD "Down" (20MHz) |
| gnd! | 11 | 0.66 | |
| Vdd! | 12 | 0.863 | |
| VCOTestOut | 18 | 3.37 | Output of VCO (20MHz, only for test) not connected with any other parts |
| VCOTestIn | 19 | 4.39 | Input of VCO (20MHz, only for test) |
| gnd! | 20 | 5.32 | |