Temperature Sensor with 10-bit SAR Analog-to-Digital Converter

Steven Pesut

Abstract

The design, simulation and layout of a 10-bit digital temperature sensor are described. The design consists of three main stages. First, there is a circuit that is sensitive to ambient temperature changes. An amplification stage then turns the output of the sensing circuit into a usable signal. Lastly, the amplified signal is fed into a 10-bit analog-to-digital converter. The ADC is a Successive Approximation Register (SAR) which utilizes an R-2R Digital-to-Analog converter to generate the digital outputs. Simulations show the sensor to have a resolution of approximately $\pm .5\ ^{o}C$ with each conversion taking approximately a minimum of 550 μs and a maximum of 1.05 ms. Test and verification procedures are outlined and described.

Contents

1 Introduction

This report describes the design, test and analysis of a temperature sensor with a 10-bit Successive Approximation Register Analog-to-Digital converter (SAR ADC). The sensor is implemented using the AMI C5N process. The circuit consists of three major stages. The first stage consists of a temperature dependent circuit. The temperature value is defined by a differential output from the stage. The second stage amplifies the differential output to improve the resolution of the device. Lastly, a SAR ADC is used to provide a 10-bit digital output that is directly proportional to the temperature.

Section 2 describes the design and analysis of the circuit, including schematics for all relevant circuitry. Section 3 shows the on-chip layout of each section of the circuit. Section 4 presents the simulations used to verify and characterize the expected device behavior. Section 5 outlines the procedures to verify the fabricated chip is working properly. Section 6 gives a summary of the project, as well as improvements for the device.

2 Circuit Design and Analysis

The circuit was designed to operate as indicated in the block diagram in Figure 1 below. The design of each of these blocks will be discussed in sections 2.1, 2.2 and 2.3 respectively.

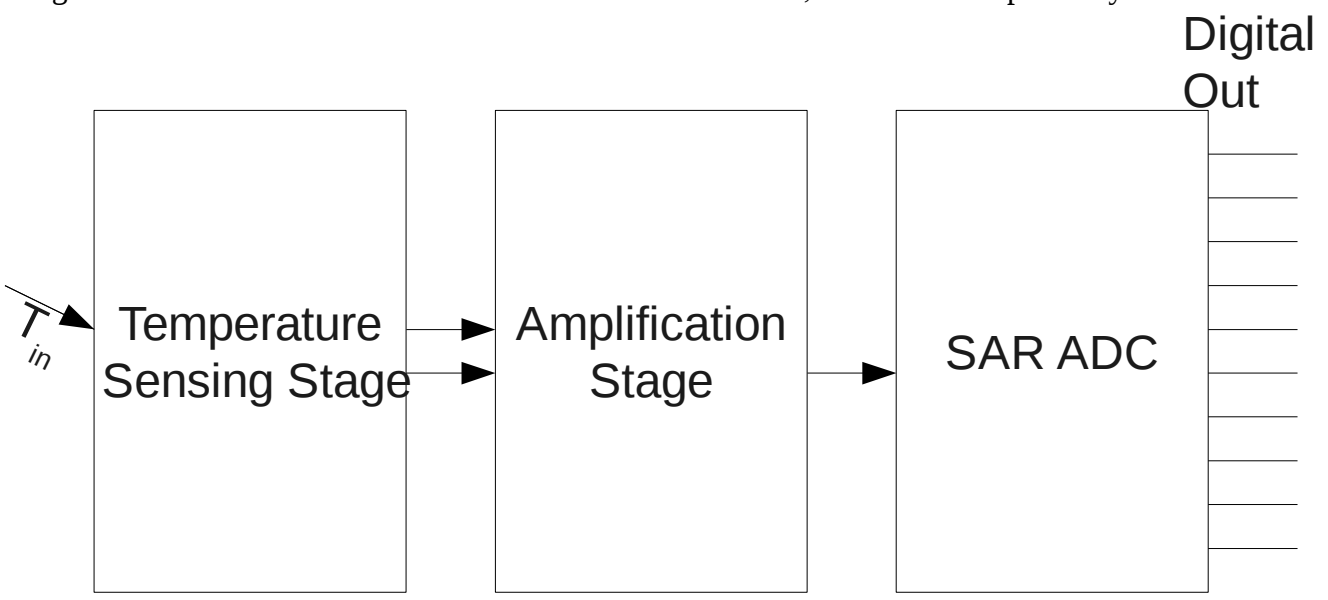

Figure 1: Block Diagram of Circuit Operation

2.1 Design of Temperature Sensing Stage

The temperature sensing circuit relies on the temperature dependence of Poly-silicon resistors. The resistors for the AMI C5N process have a tolerance of 2000 ppm, or .2% per ºC. All bodies in the circuit are tied to the source to eliminate the body effect on V_t. This causes the mirrored currents to be more constant as temperature changes. The circuit schematic for the temperature sensing stage can be seen below in Figure 2.

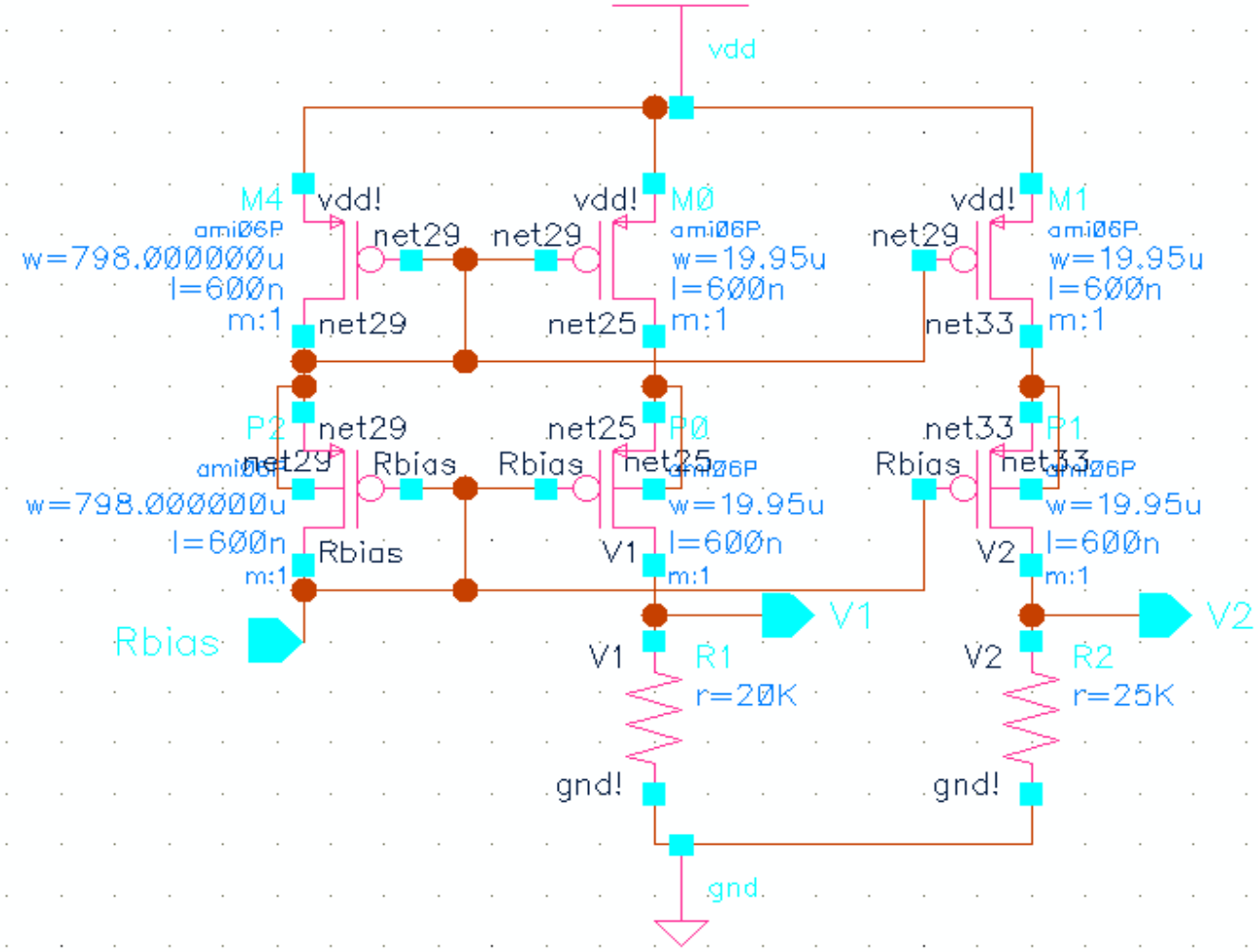

Figure 2: Temperature Sensing Circuit

This circuit operates by generating a bias current in the left-most branch. This bias current is mirrored to the other two branches to create a current of 100 uA through the 20 kΩ and 25 kΩ resistors. With the resistors varying at approximately .2% per ºC, this causes the voltage difference between V1 and V2 to change at 1 mV per ºC. The bias resistor is broken out on one pin of the chip to mitigate the

temperature dependence of that component. This enables the current mirror to be held at a more constant current as the temperature changes. Two versions of the current source were designed. The design shown above uses a relatively high bias current (4 mA). The second design has a bias current of 100 µA, which reduces the power dissipation of the circuit. The currents mirrored through the resistors is set to 100 µA for both designs.

2.2 Design of Amplification Stage

The differential signal from the temperature sensor is then amplified into a signal analog signal that can be fed into the Analog-to-Digital converter. The amplification stage consists of two amplifiers. The first is a differential amplifier that increases the amount of gain on the signal for each ºC of temperature change. Since the resistance increases as temperature decreases, this gives the largest voltage difference at the lowest temperatures. This would cause the ADC to give higher readings at lower temperatures. This is corrected in the amplification stage using an inverting operation amplifier. This second stage not only flips the signal, but also adds more gain to the signal. The final signal provides approximately 20 mV of difference per ºC. The schematic of the amplification can be seen below in Figure 3.

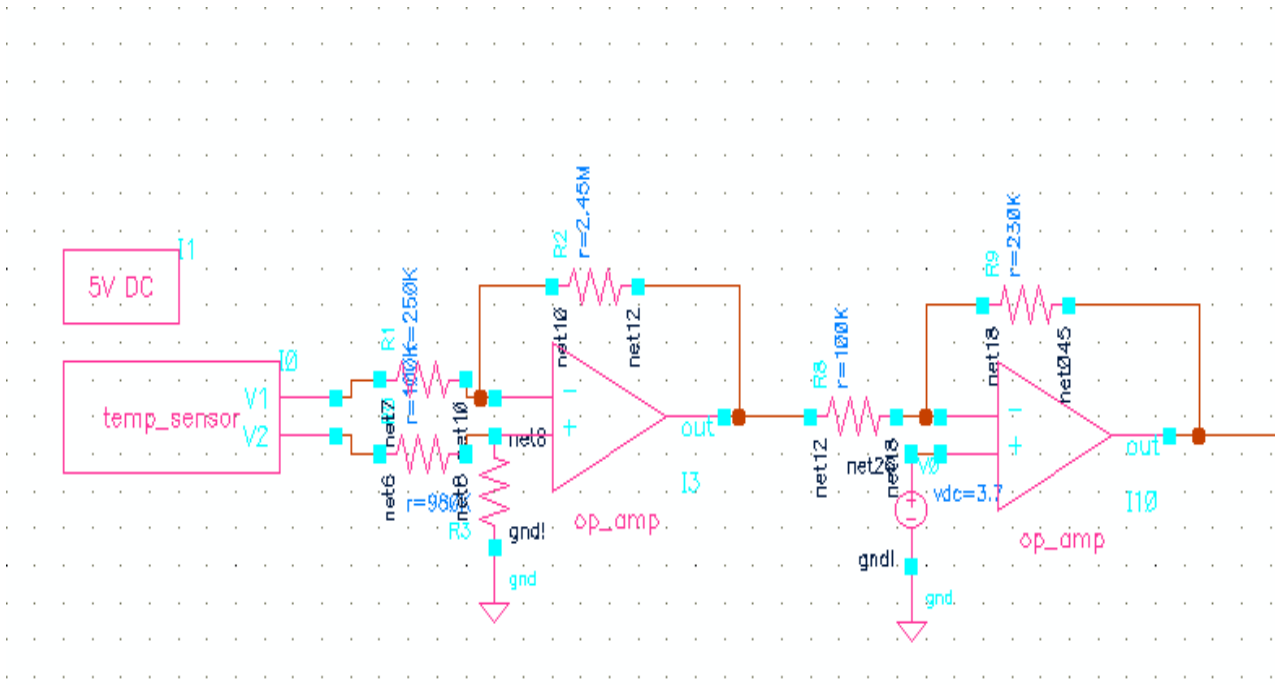

Figure 3: Amplification Stage

The operational amplifiers used in the design have very basic requirements. Significant temperature changes occur at a very low frequency, and the largest gain above is 9.8. An amplifier that has a gain of 20+ dB at frequencies below 100 Hz are more than sufficient for the task. For this reason, a simple two-stage amplifier was designed. The design consists of a differential pair stage followed by a common source stage at the output of the amplifier. A Miller capacitor is added between the common source input and output. This increases the phase margin of the amplifier. The schematic of the amplifier is shown below in Figure 4.

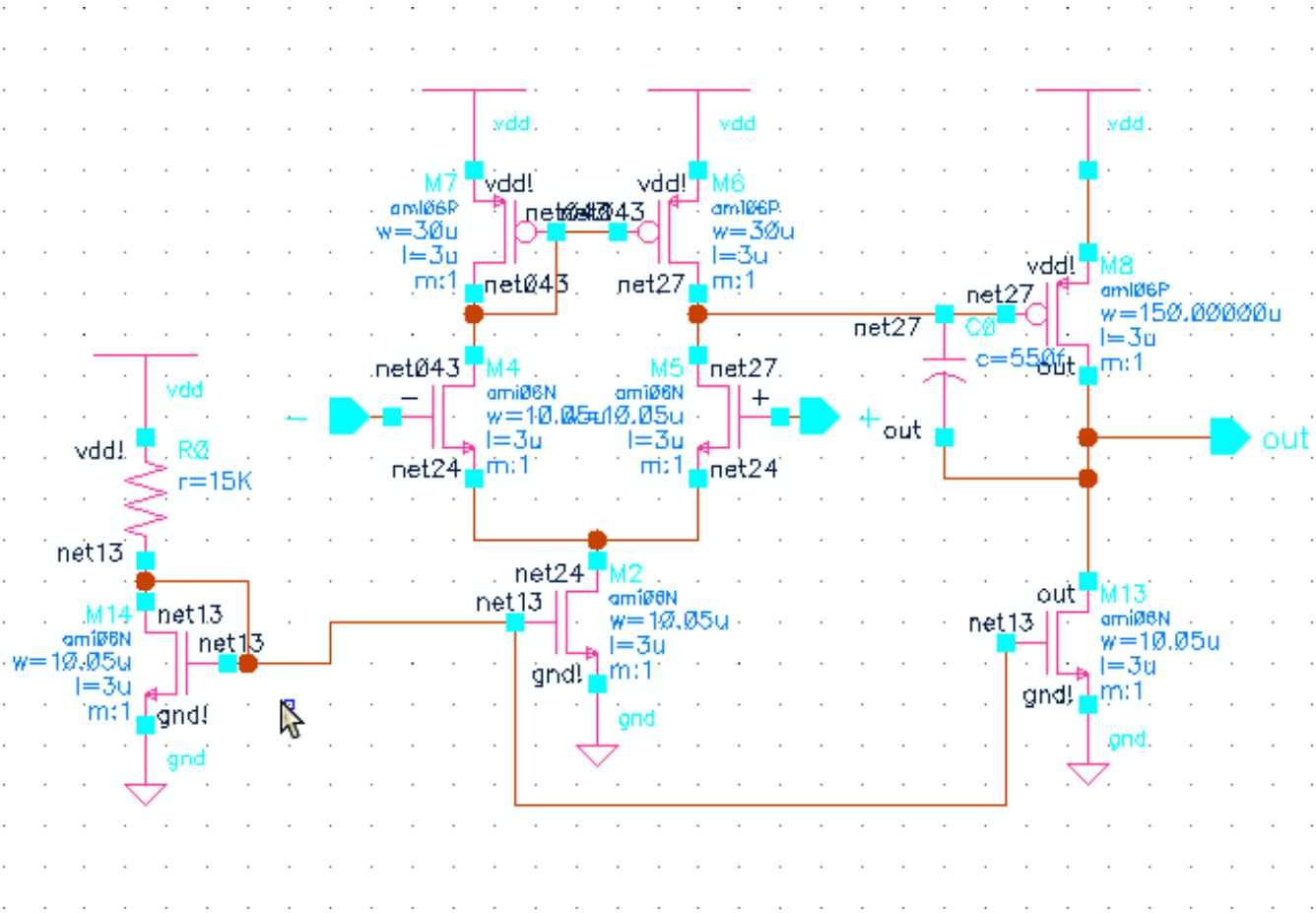

Figure 4: Operational Amplifier Schematic

2.3 Design of Analog-to-Digital Converter

The Analog-to-Digital converter is implemented using a Successive Approximation Register for all conversions. This design was chosen because it requires minimal logic and space on the chip. The design operates in the following way. A 10-bit register is setup to hold the digital value of the conversion. These 10 bits are fed into a Digital-to-Analog converter. The output of the DAC is fed into a comparator. The comparator also has the output of the amplification stage fed into it. Depending on the output of the comparator, a logic block flips the appropriate bit in the register to high or low. The bits are selected one at a time and changed if necessary. A conversion is complete once all bits have been adjusted appropriately, giving the correct digital value for the analog output of the amplification stage. The final digital values are then clocked to a register of D Flip Flops which are tied to output pins of the chip. The operational amplifier design from the amplification stage is used here as the comparator. The other two blocks of the SAR ADC will be discussed in the following sections. A block diagram overview is shown below in Figure 5.

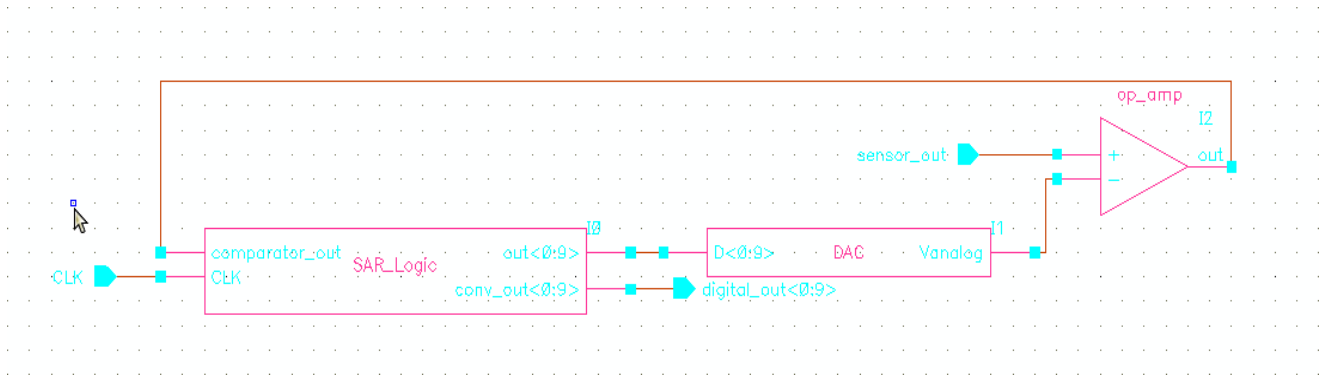

Figure 5: Block Diagram of SAR ADC

2.3.1 Design of Digital-to-Analog Converter

The DAC is designed as a simple R2-R network. Inputs are taken from the 10-bit register. These inputs are used to select whether bits in the DAC are set to V_{dd} or ground. For the DAC, R = 100kΩ. The schematic design is shown below in Figure 6.

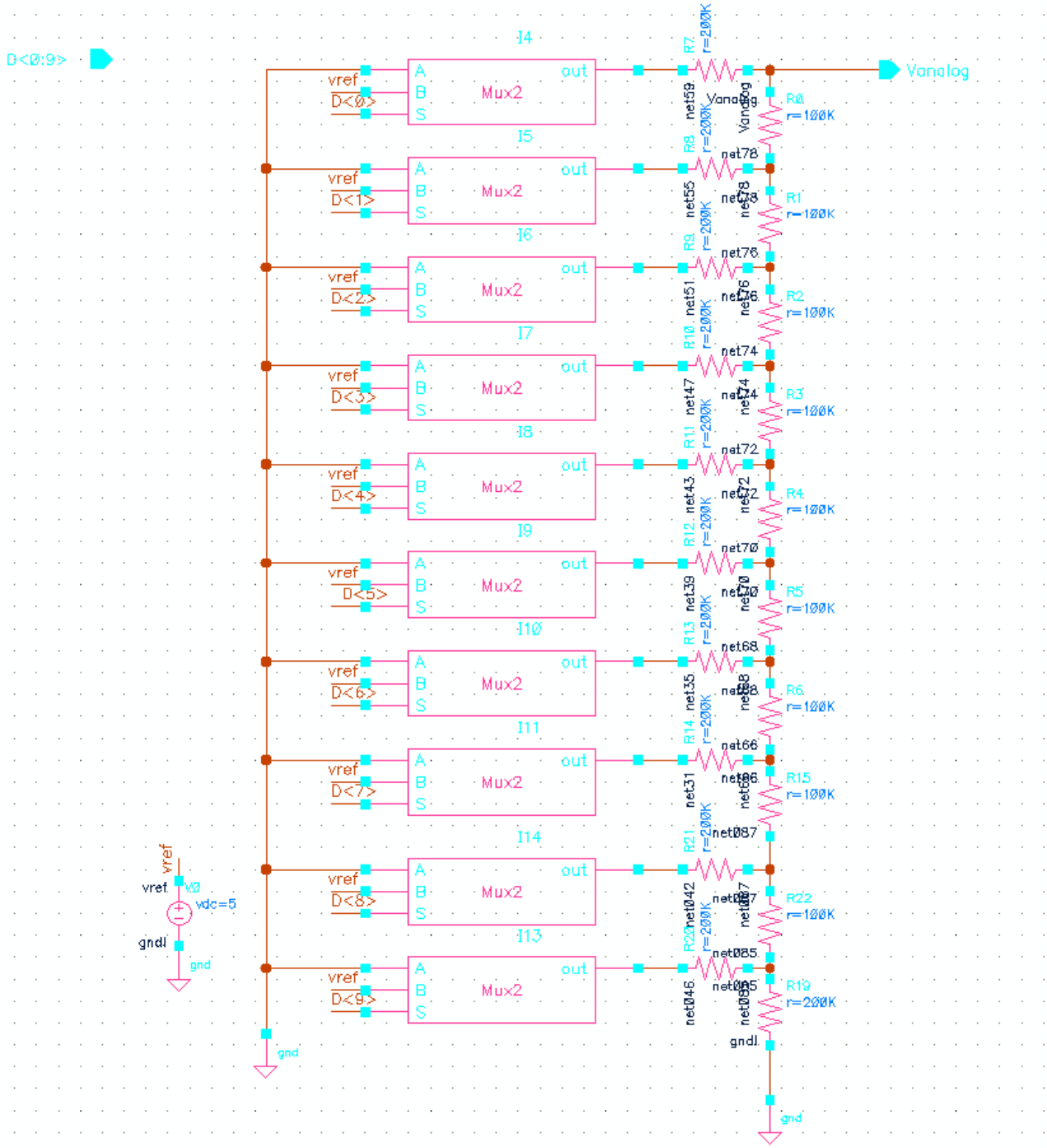

Figure 6: Digital-to-Analog Converter Schematic

2.3.2 Design of SAR Controller Logic

The logic controller takes the comparator output and a clock signal as inputs. The controller starts every conversion by zeroing out all of the bits in the 10-bit register. These bits are then flipped high one at a time – most significant to least significant. This is accomplished with a shift register. The shift register generates select lines for ten multiplexers. The shift register ensures that only one select line is high at any given time throughout the conversion. A series of D flip flops is used to move the select line one bit per clock. These multiplexers select whether the previous bit state, or the comparator output is fed into the 10-bit register. The process is demonstrated on one bit below in Figure 7.

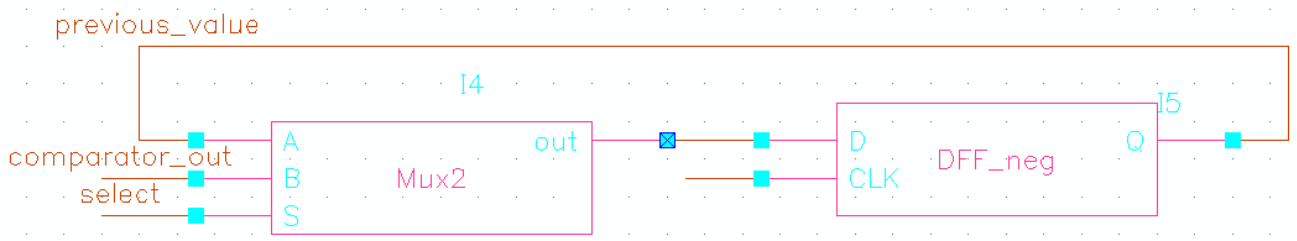

Figure 7: Register Bit-flipping Process

The controller flips one bit high and checks if the comparator reads low (value is too large). If the comparator reads low, the bit must be flipped back to its original low state. To flip the bit back to its original state, the clock into the shift register must be blocked. This keeps all select lines at the same value for an extra clock cycle, which flips the bit back to its previous state. This is accomplished with the following logic seen in Figure 8.

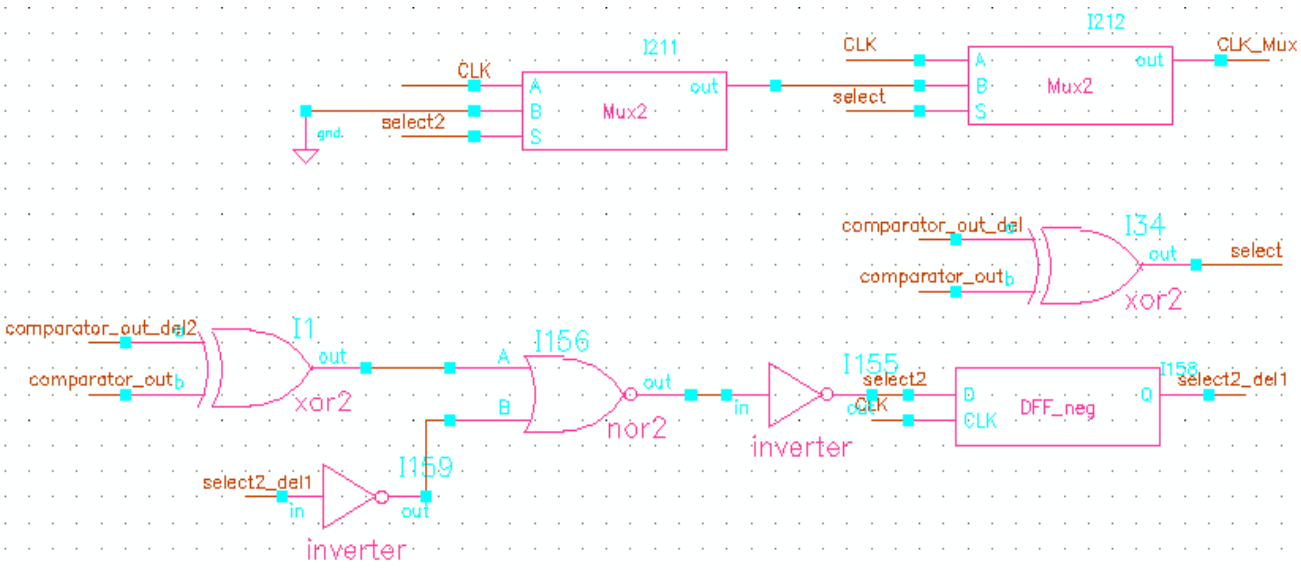

Figure 8: Clock-Blocking Logic

The converter then moves on to the next bit until all bits have been set appropriately. Once the final value is reached, the bits are written to an output register, and are reset to perform the next conversion. The outputs are pinned out of the chip and can be read with a microcontroller or logic analyzer. A simulation of the SAR ADC is shown on the next page in Figure 20. The DAC output is the blue line. It approaches the green line (simulated output of amplification stage). When all 10 bits have been stepped through, the digital outputs update.

A simple ring oscillator designed to have an operating frequency of approximately 20 kHz is used to clock the ADC. This frequency will fluctuate with temperature. This is not an issue, because the converter does not require a specific frequency to operate. Conversion times will change depending on on the temperature.

3 Design Layout

All design layout was performed using the Virtuoso layout editor in the Cadence design suite. Layouts were designed to minimize device size as well as enable easy wire routing for the design.

3.1 Layout of Temperature Sensing Circuit

Both sensing circuits (high current and low current) were laid out to minimize the footprint on the chip. The layout of the higher current circuit can be seen in Figure 9.

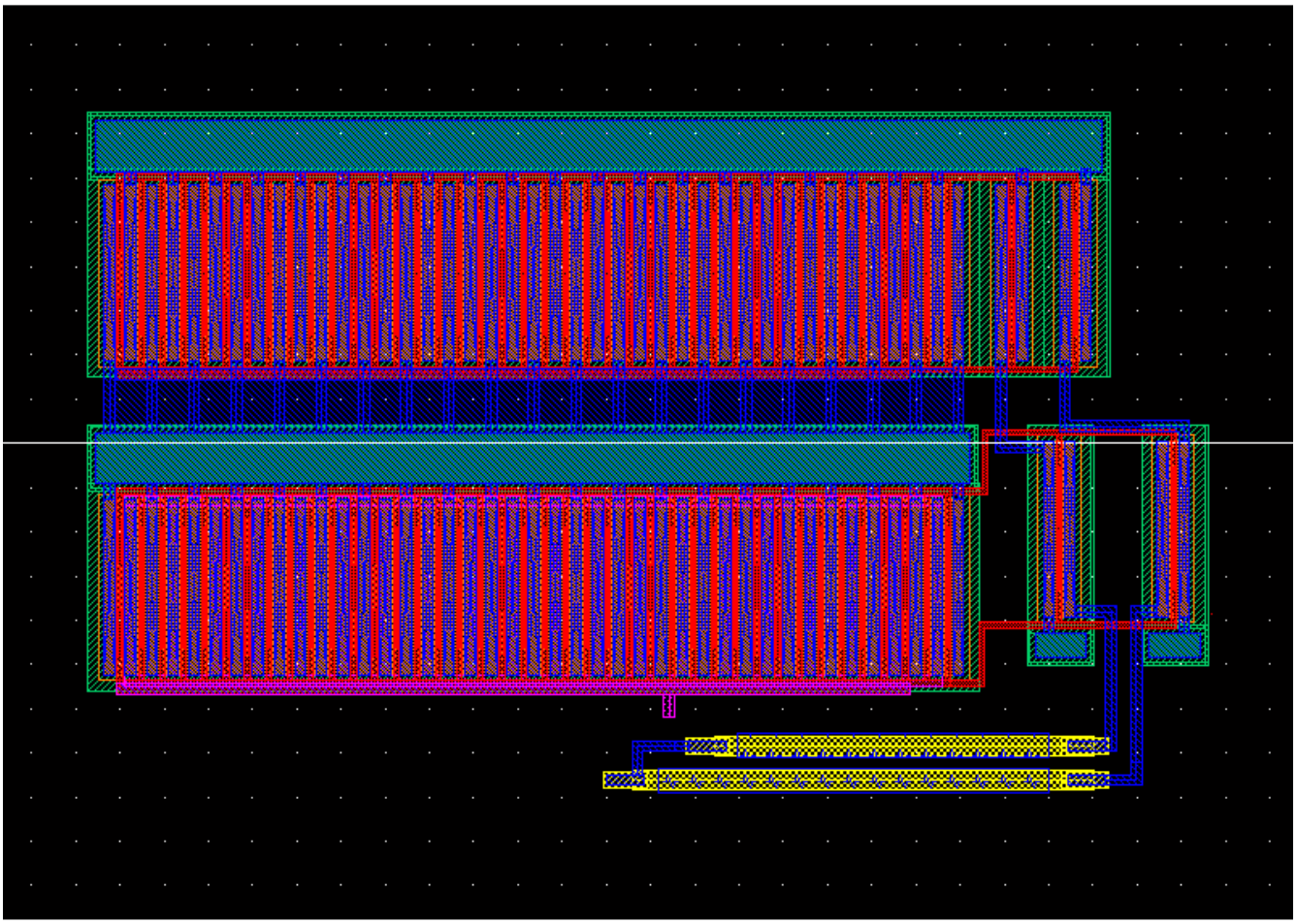

Figure 9: Layout of Temperature Sensing Circuit

3.2 Layout of Amplification Stage

The building block of the amplification stage is the operational amplifier. The layout is shown below in Figure 10.

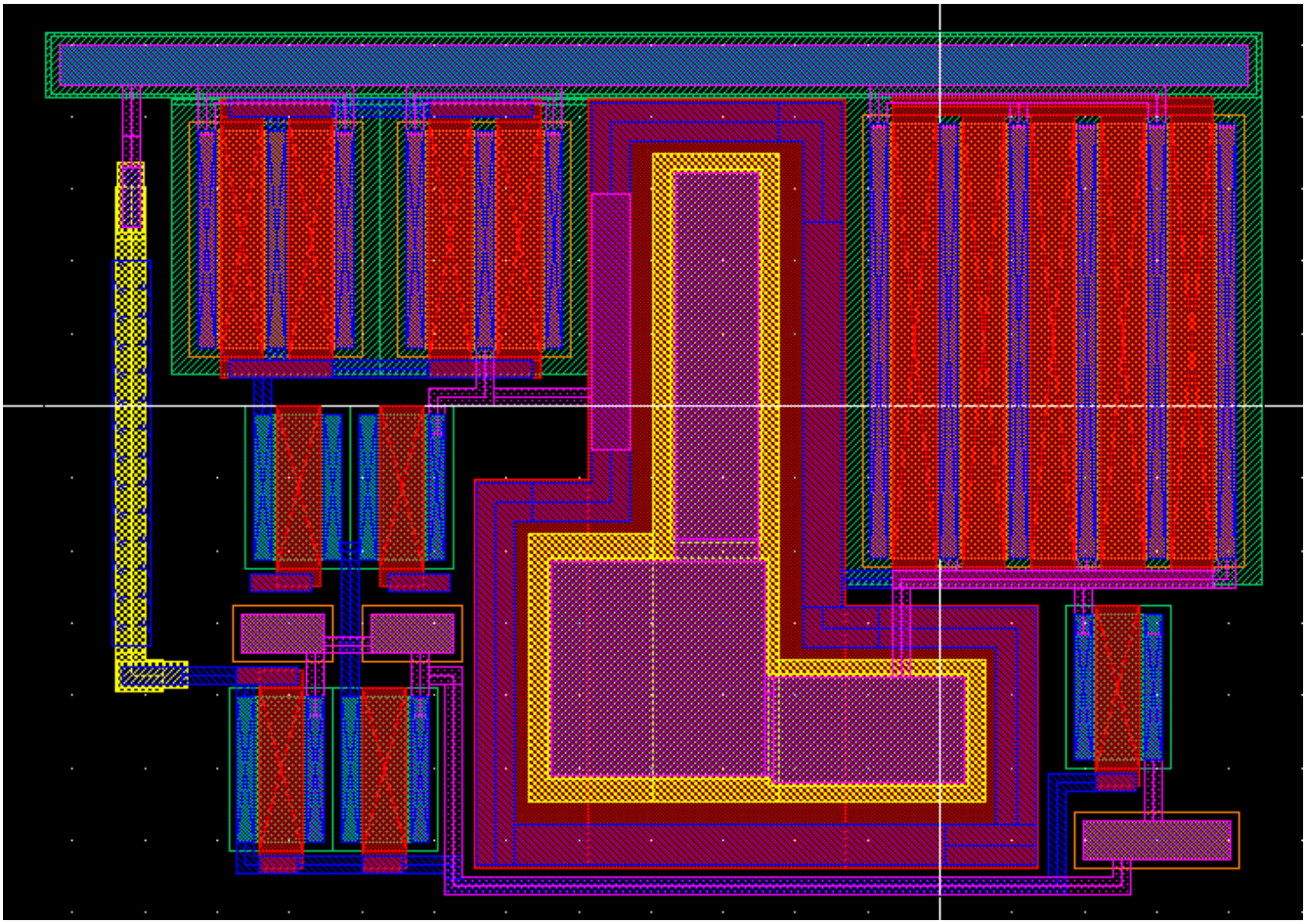

Figure 10: Layout of Operational Amplifier

These necessary resistors were added around the amplifiers to complete the stage. The resistors were laid out in such a way as to fit closely with other stages, which allowed for a minimum size design. The amplification stage layout can be seen below in Figure 11.

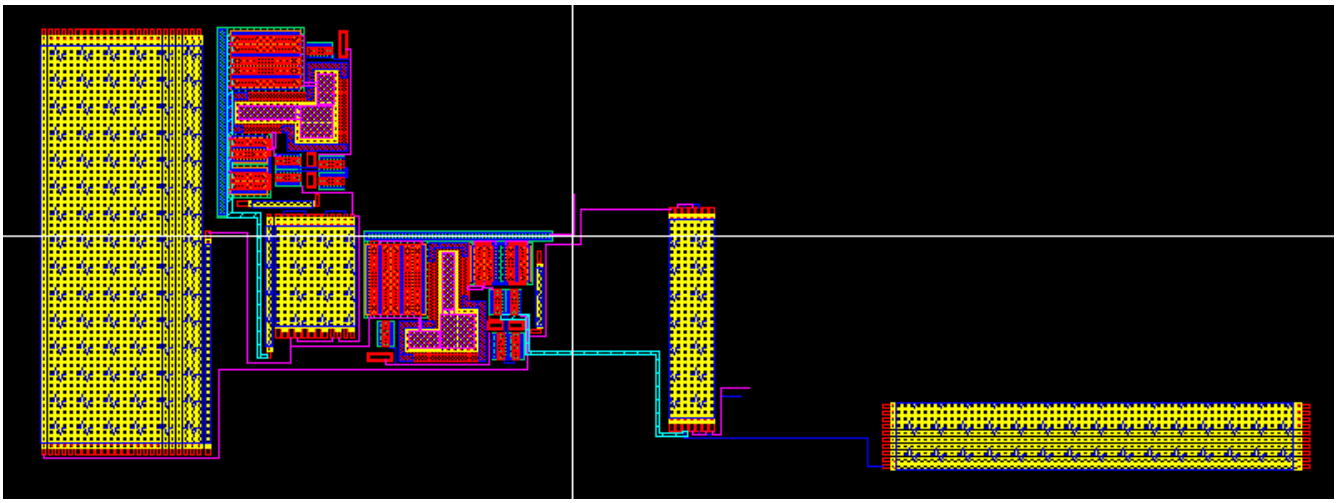

Figure 11: Layout of Amplification Stage

3.3 Layout of SAR Analog-to-Digital Converter

The SAR ADC was laid out in such a way that area was minimized. The minimal layout of this section allowed for two sensors to be put on each chip. The layout of the ADC can be seen below in Figure 12.

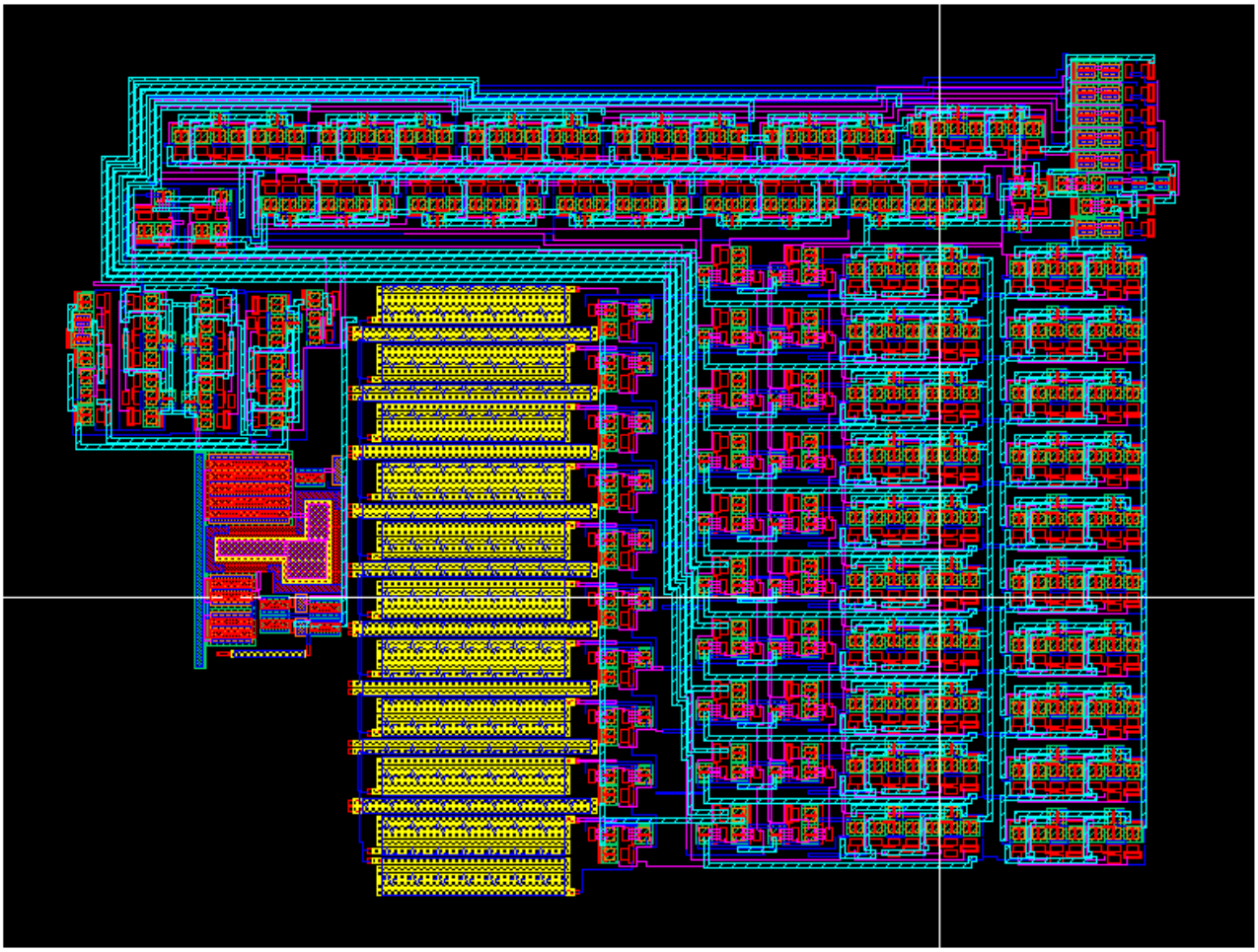

Figure 12: Layout of SAR ADC

3.4 Completed Layout

The final layout can be seen below in Figure 13. The lower half of the layout is the low-current sensor and the upper half is the high-current sensor.

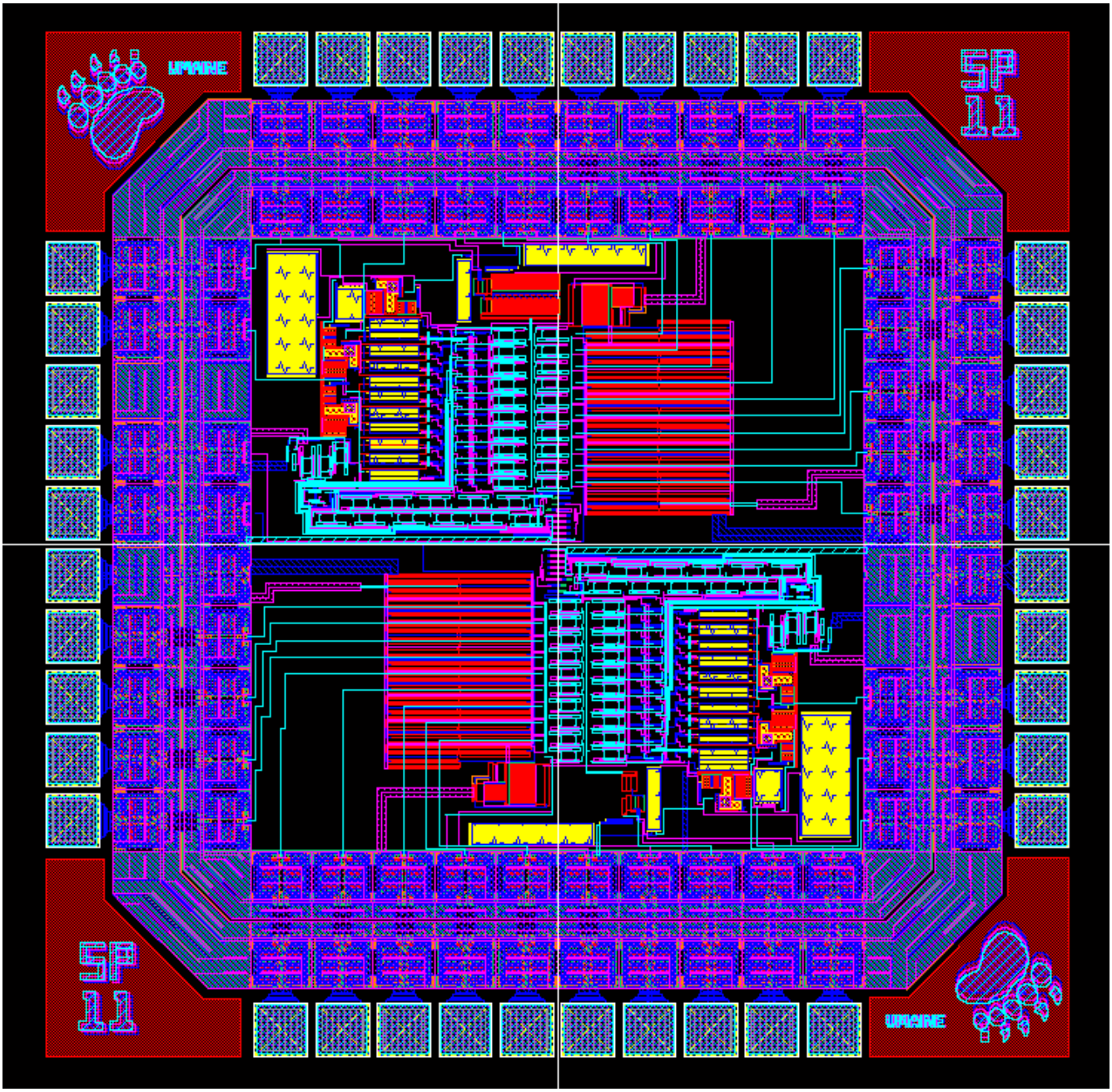

Figure 13: Complete Layout of the Chip

4 Circuit Simulation

All individual sections of the circuit were simulated and verified separately before being combined for the total simulation. The temperature sensing and amplification stage were combined into the first simulation and the SAR ADC was simulated next. The complete circuit was then simulated and characterized. Each of these simulations will be discussed in the following sections.

4.1 Temperature Sensing and Amplification Verification

The first portion of the circuit that must be analyzed is the operational amplifier. The amplifier must have a gain greater than 20 dB at low frequencies while having an acceptable phase margin. The simulation below in Figure 14 shows a low frequency gain of 29.81 dB and a phase margin of 29.1º. The amplifier meets the necessary specifications.

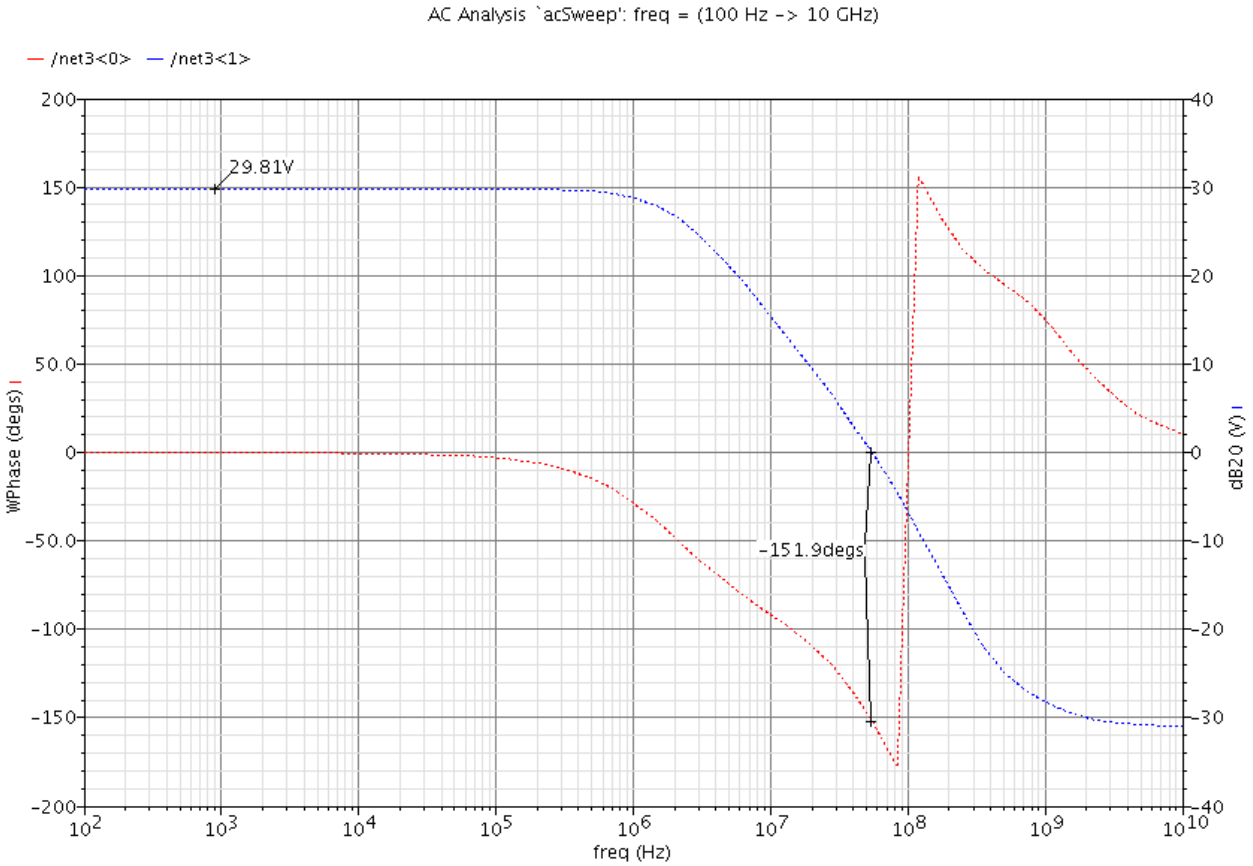

Figure 14: Simulation of Op Amp Characteristics

Voltages were measured from the output of the amplification stage every 10 ºC from -30 ºC to 100 ºC. These values were plotted and fit with a line of best fit. The result is a very linear relationship between the output voltage of the amplification stage and the temperature. The graph is shown below in Figure 15.

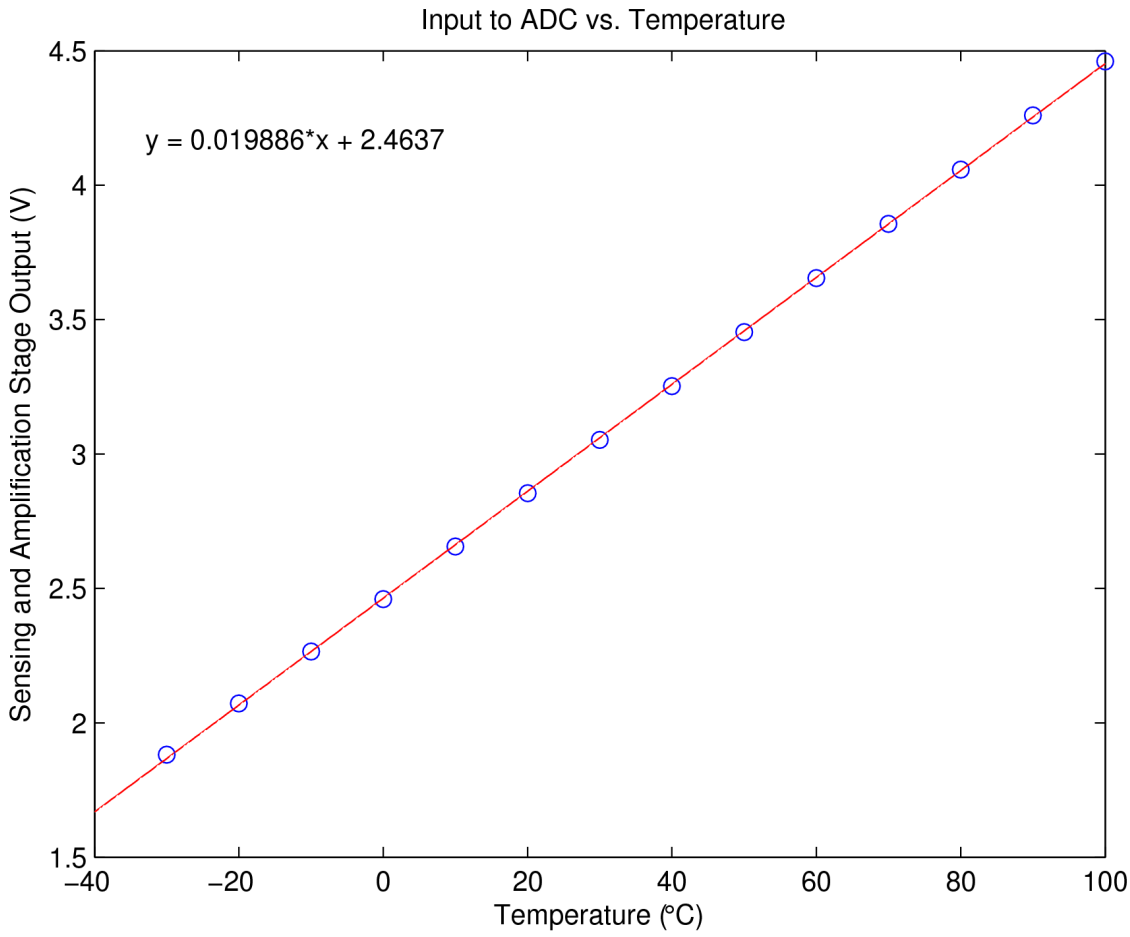

Figure 15: Output of Amplification Stage vs. Temperature

4.2 Analog-to-Digital Converter Simulation

The following simulation shows the performance of the ADC. A 20 kHz clock was used to drive the simulation. The green line shows the target voltage level that represents the voltage generated by the temperature sensing and amplification stages. The blue line shows the output of the DAC. It can be seen that only one bit is adjusted per clock cycle until all 10 bits have been cycled through. In the simulation the conversion is complete at .75 ms, and the digital output signals (red line) have been updated.

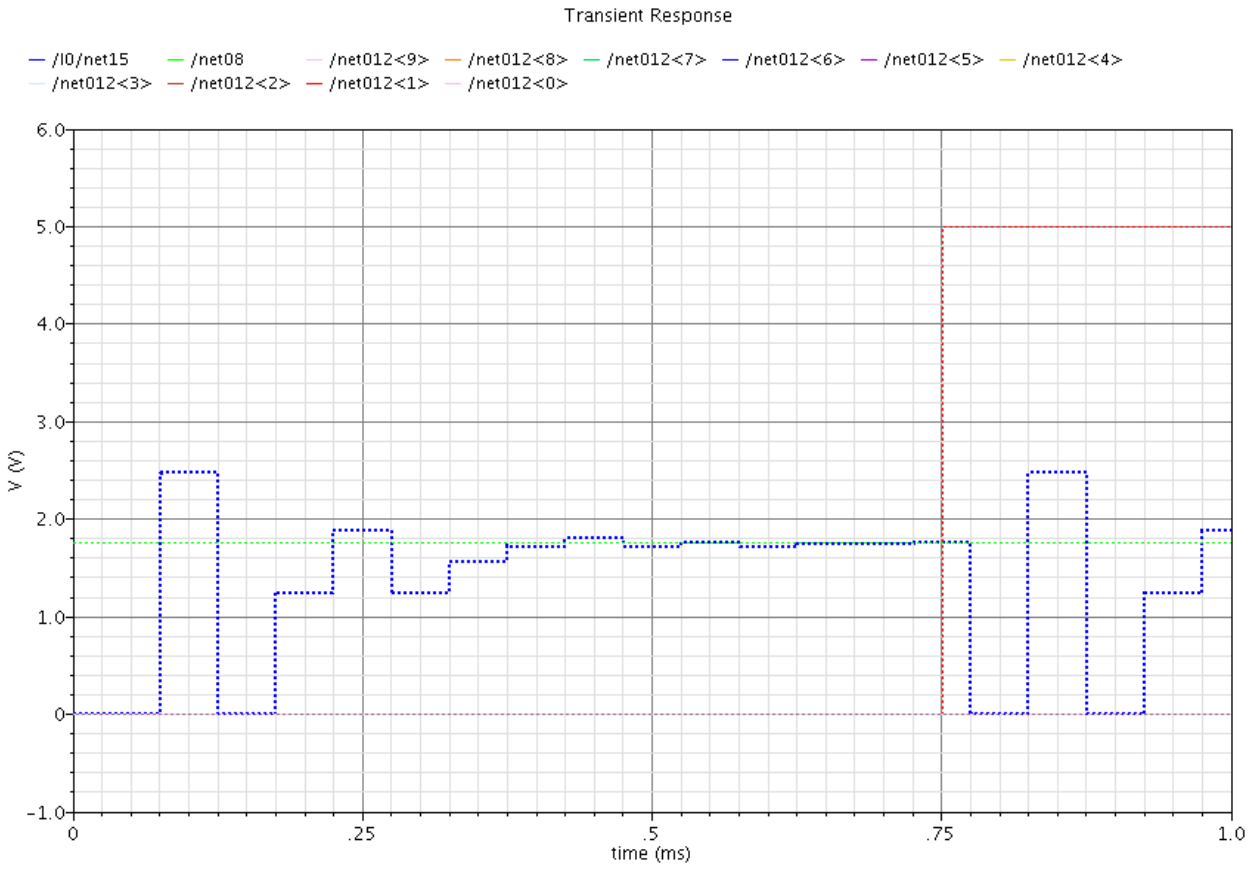

Figure 16: Simulation of SAR ADC

4.3 Full Circuit Simulation

Simulations of the circuit were run every 10 °C from -30 °C to 100 °C. The digital output values were taken at each of these points and converted to a decimal value. The data was plotted in Matlab and characterized using a linear fit. The resulting graph gives a characterization of the device for all temperature values within range. This graph is shown in Figure 17.

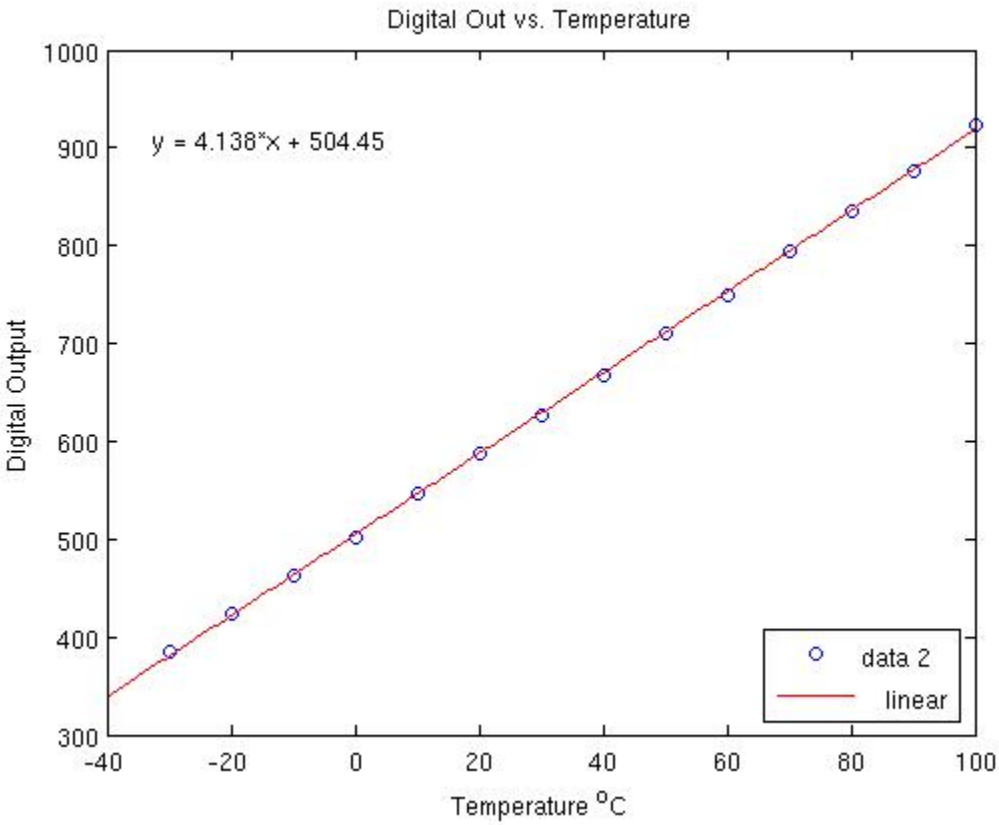

Figure 17: Simulated Digital Output vs. Temperature

From the line of best fit equation, the sensor has a simulated maximum error of ±.5 °C and a resolution of ±.25 °C.

5 Test and Verification of Device

The device has been laid out such that there are several ways of verifying the performance of the circuit. The pin mapping for the device can be seen below in the following table. Note: pins 1-19 refer to the high-current design and pins 20-40 refer to the low-current design.

Table 1: Pin Connections for the Chip

Pin Number	**Pin Function**	**Pin Number**	**Pin Function**
1	Digital Out[0]	21	Vdd
2	Digital Out[1]	22	Digital Out[0]
3	Digital Out[2]	23	Digital Out1[1]
4	Digital Out[3]	24	Digital Out1[2]
5	Digital Out[4]	25	Digital Out1[3]
6	Digital Out[5]	26	Digital Out1[4]
7	Digital Out[6]	27	Digital Out1[5]
8	Digital Out[7]	28	Digital Out1[6]
9	Digital Out[8]	29	Digital Out1[7]
10	Digital Out[9]	30	Digital Out1[8]
11	Ring Oscillator Post-Buffer	31	Digital Out1[9]
12	Bias Resistor Pin	32	Ring Oscillator Post-Buffer
13	Voltage Bias for Amplification Stage	33	Bias Resistor Pin
14	Voltage V2 from Temperature Sensing Stage	34	Voltage V2 from Temperature Sensing Stage
15	Voltage V1 from Temperature Sensing Stage	35	Voltage V1 from Temperature Sensing Stage
16	Output from first amplifier of the Amplification Stage	36	Voltage Bias for Amplification Stage
17	Input to the ADC	37	Output from first amplifier of the Amplification Stage
18	NC	38	Input to the ADC
19	Ring Oscillator Pre-Buffer	39	NC
20	Ring Oscillator Pre-Buffer	40	Ground

Several of the output pins can be used to verify each section of the circuit. Debugging instructions for each block of the circuit will be presented in the following sections.

5.1 Temperature Sensing Circuit Verification

The biggest downfall of the temperature sensing circuit is its reliance on the resistor values. Although resistors were laid out to have the correct value, it is likely that the resistors on chip will not be at the designed values. This is due to process variation. If initial resistor values are incorrect, the differential voltage output will be incorrect. This will lead to incorrect measurements. As a means of counteracting this error, the bias resistor has been broken off of the chip, to allow for the current to be tweaked. The procedure to determine this resistor value is as follows.

1. Set the bias resistor to its calculated value

   R_{bias} = 618 Ω (high current) or R_{bias} = 24.8 kΩ (low current)
2. Measure voltages V1 and V2
3. Adjust the value of R_{bias} until V1 = 2V and V2 = 2.5V (Assuming Temp = 27 ºC)

Once V1 and V2 are appropriately set, the temperature sensing circuit has been setup.

5.2 Amplification Stage Verification

There should be few errors present in the amplification stage. The first amplifier in the stage should have no issues. The gain should be largely independent of process variation since all resistor ratios should be preserved. This amplifier can be verified by reading the output of pin 16 (high current) or 37 (low current). A differential gain of 9.8 is expected.

Some amount of tweaking can be performed on the second amplifier in the stage. The V_{bias} of the inverting amplifier is external to the chip. This value can be adjusted to get the expected value at the end of the amplification stage. The following procedure can be used to adjust the output of the amplification stage.

1. Verify the operation of the first amplifier by measuring the two inputs, V1 and V2, and the output.
2. Measure the output of the amplification stage. Adjust the external voltage supply to get the correct input to the ADC. The input value can be found using the following equation.

$$\text{Input} = (.019886*\text{Temp} + 2.4637)\ \text{V}$$

5.3 SAR Analog-to-Digital Converter Verification

There are a limited number of way to debug the SAR ADC due to pin limitations. The procedure to setup the SAR ADC and take measurements is given below.

1. The ring oscillator may need to be started up manually. Measure pin 11 and 32 with an oscilloscope. If the oscillator is working properly skip step 2.
2. The ring oscillator was unable to start without initial conditions. To provide the initial conditions, tie pin 19 and 20 to ground momentarily. Remove the ground connection, and repeat step 1.
3. Measure the analog input to the converter (pins 17 and 38) as well as the digital output pins. The expected digital value can be found using the following equation.

$$\text{Digital\_Out} = 4.138*\text{Temp} + 504.45$$

The measurements resulting from this procedure will be compared to simulated data once the fabricated chips have been tested. This report will be revised once these comparisons have been made.

6 Summary and Conclusion

The design, simulation and layout of a 10-bit digital temperature sensor was described. The design included a circuit sensitive to ambient temperature, an amplification stage that generated a usable input to the ADC and a SAR ADC that gave a 10-bit digital output. Experiment procedures were outlined. Results are forthcoming, but simulations show the sensor to have a resolution of approximately $\pm.25$ ºC with an maximum error of $\pm.5$ ºC. Each conversion took an approximate minimum 550 μs and an approximate maximum of 1.05 ms. Test and verification procedures were outlined and described.

6.1 Suggestion for Future Work

Currently, the biggest drawback of this device is the number of I/O pins required to get a temperature reading. It takes a minimum of 10 pins on a microprocessor to get a valid reading. A state machine could be added that responds to the I^2C protocol. Only two pins would be required if this were implemented.

Aside from the number of input pins, simulations indicate this device should operate inline with many commercially offered sensors in terms of conversion time, resolution and accuracy.

6.2 Biography

Steven Pesut grew up in Crouseville, Maine. He graduated from Washburn District Hight School in Washburn, Maine in 2007. He is currently completing his Bachelor's degree in Electrical and Computer Engineering at the University of Maine and will be graduating in May 2011. He will be working at Analog Devices, Inc. as a product test engineer starting Summer 2011.

7 Appendix

7.1 Schematics

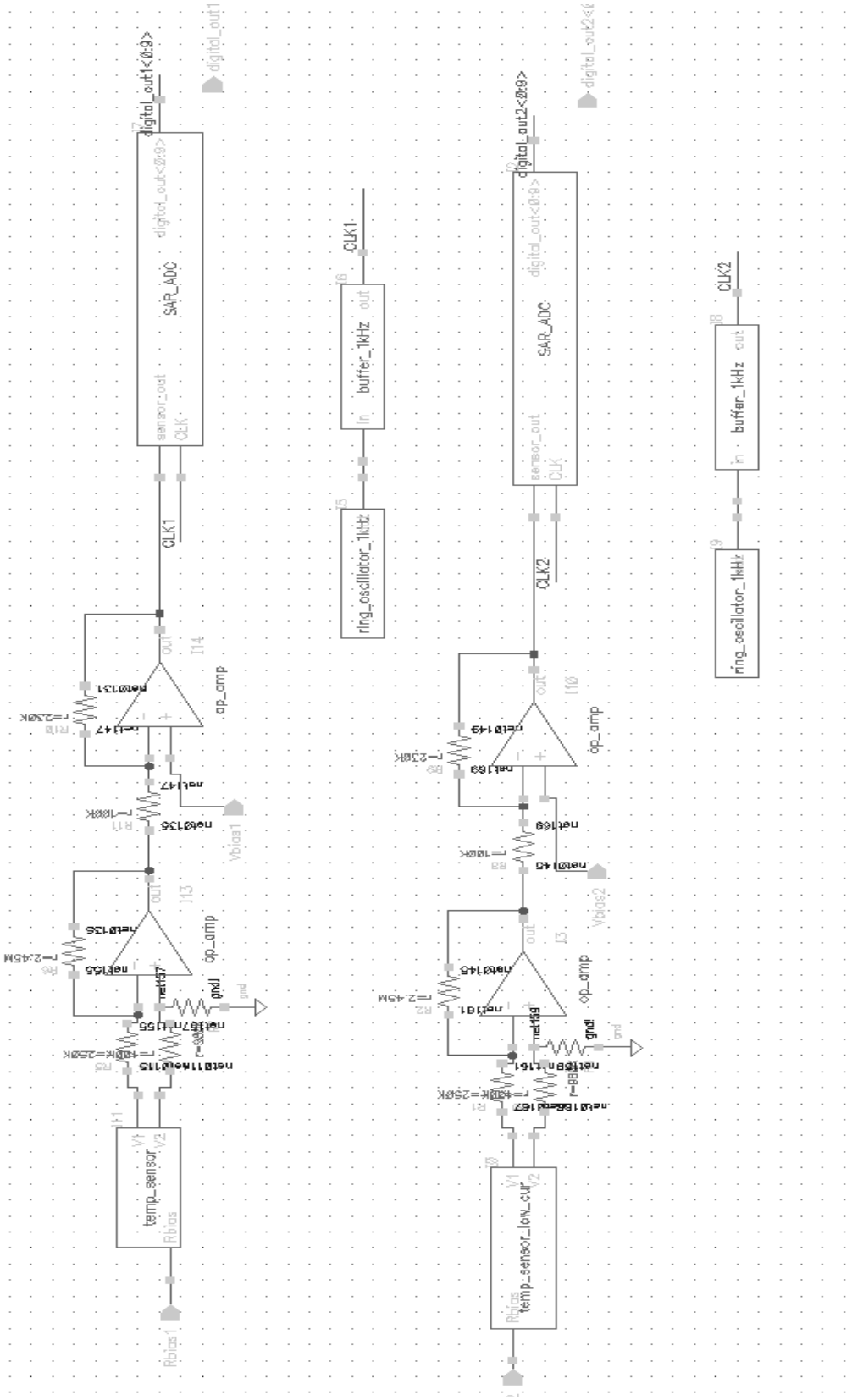

Figure 18: Top-level Design Schematic

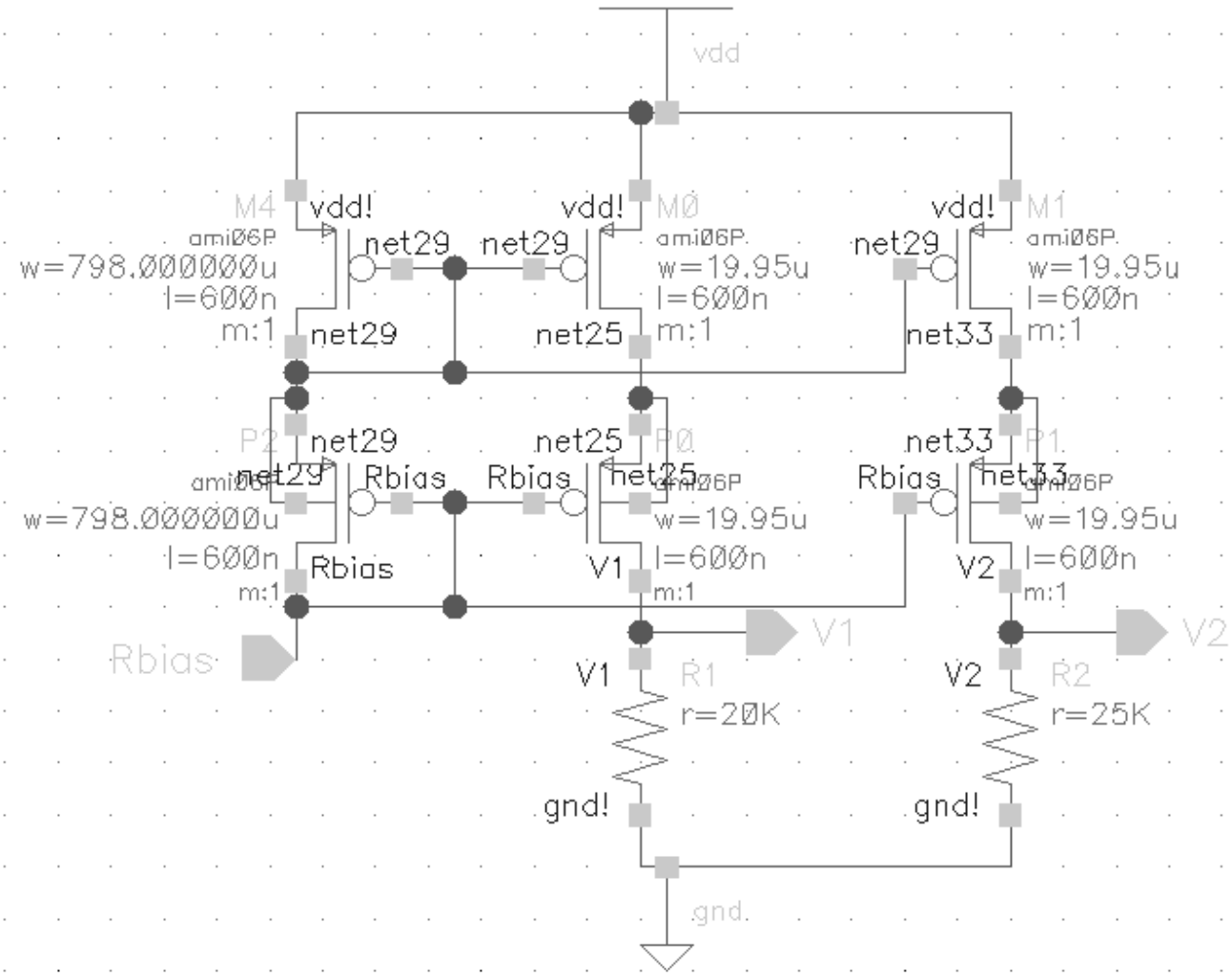

Figure 19: Temperature Sensing Circuit Schematic

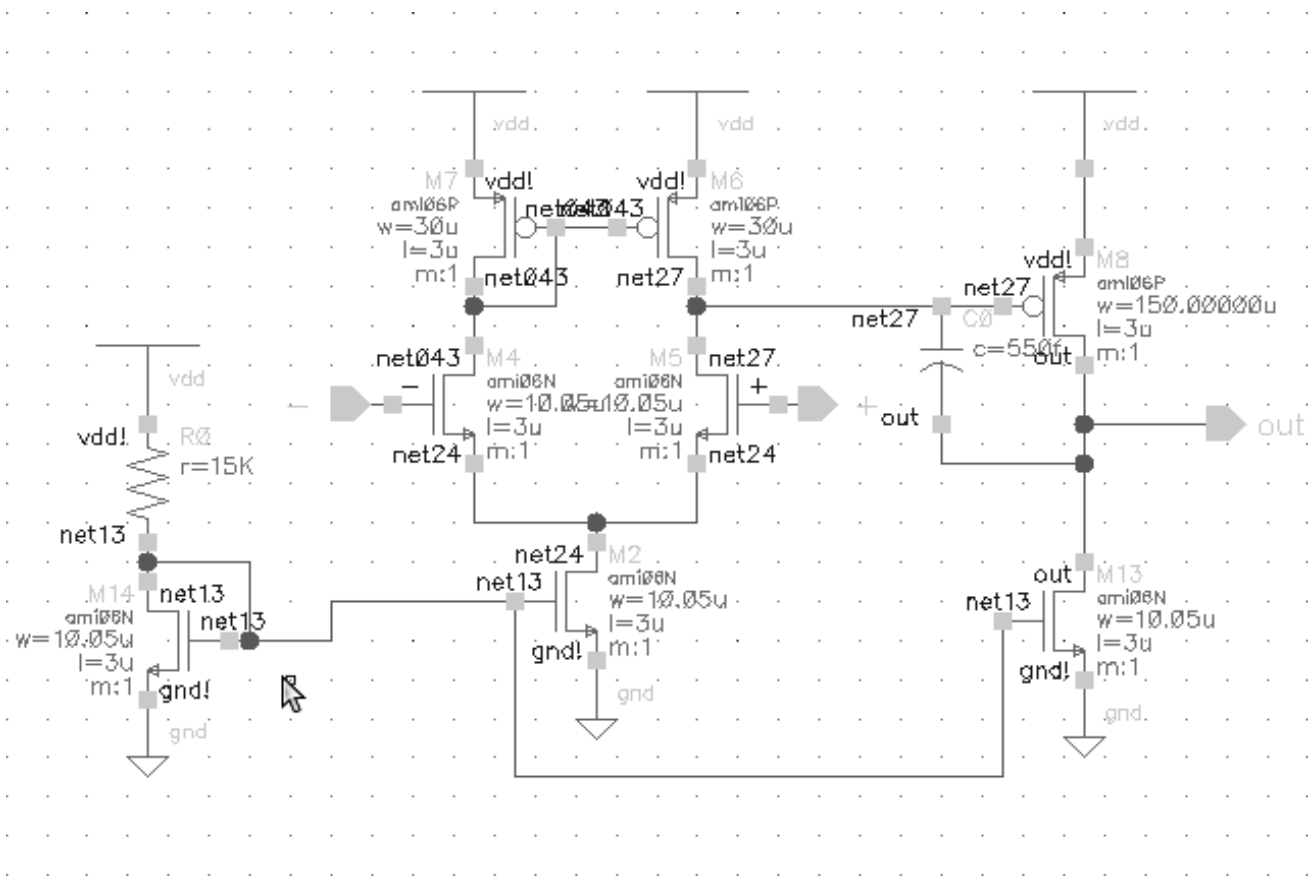

Figure 20: Operational Amplifier Schematic

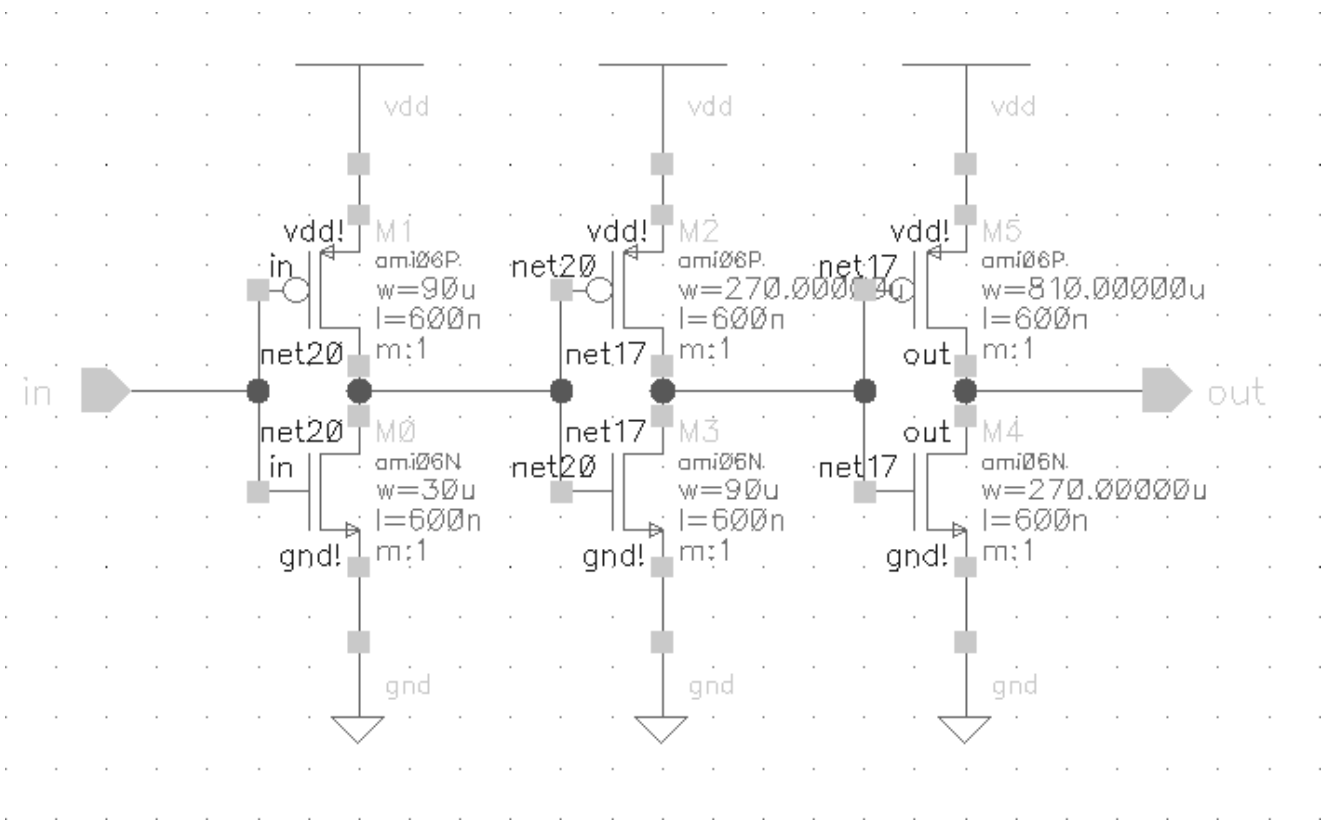

Figure 21: Three-Stage Digital Buffer Schematic

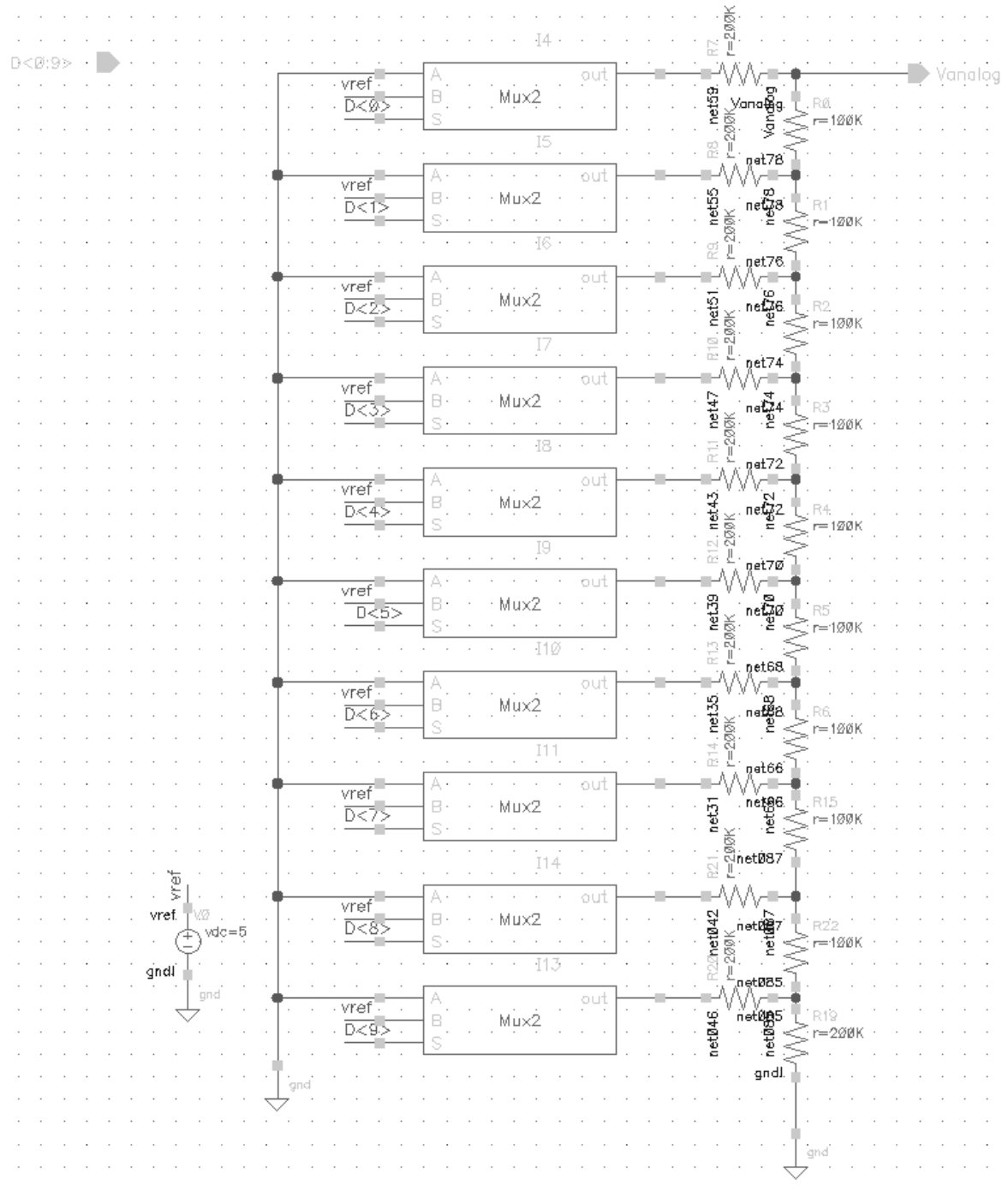

Figure 22: R2-R Digital-to-Analog Converter Schematic

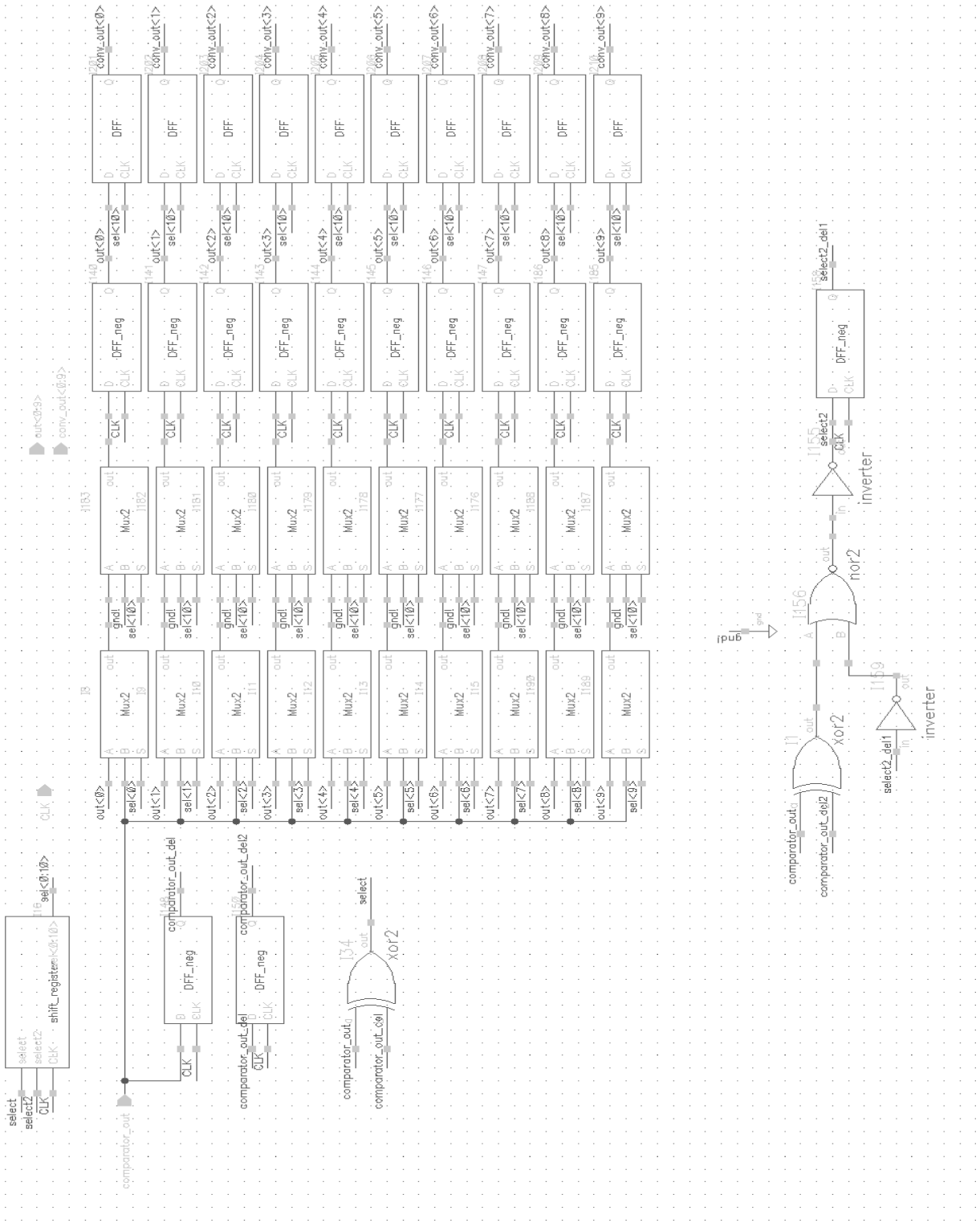

Figure 23: SAR Logic Block Schematic

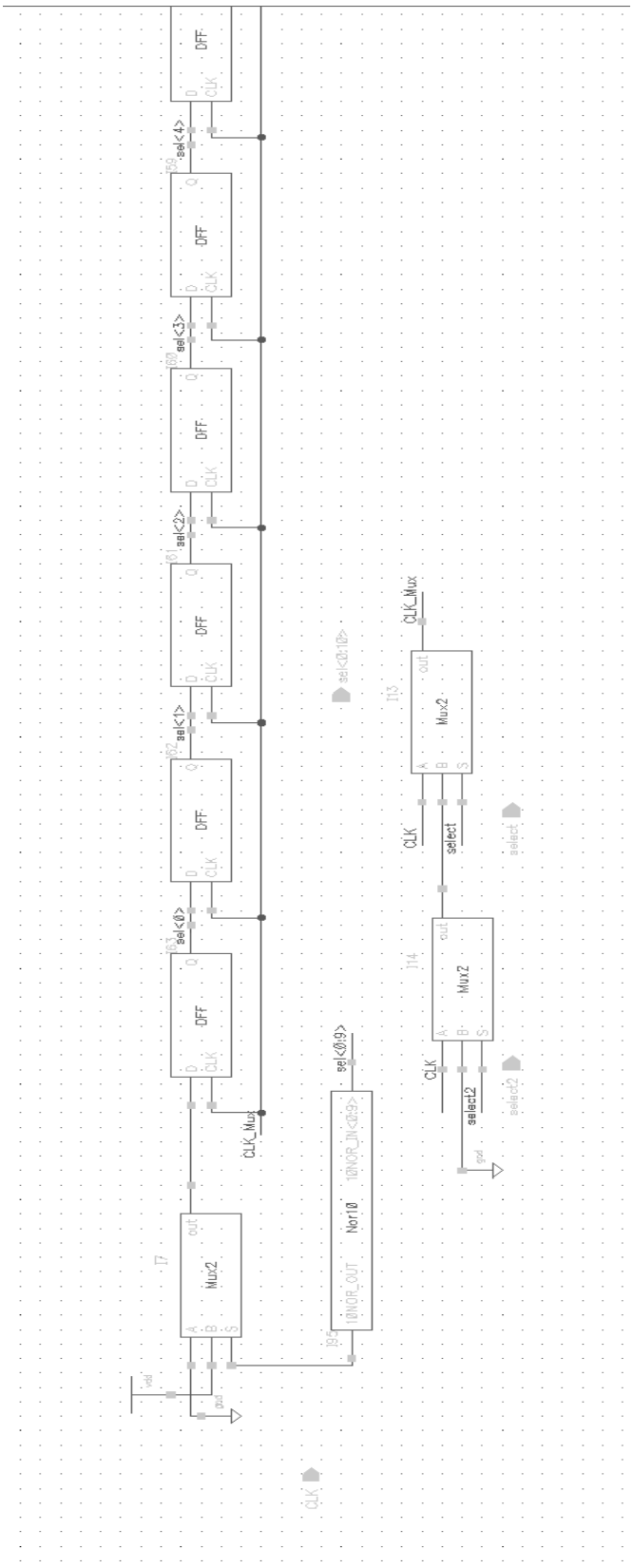

Figure 24: Shift Register Schematic

7.2 Final Circuit Layout

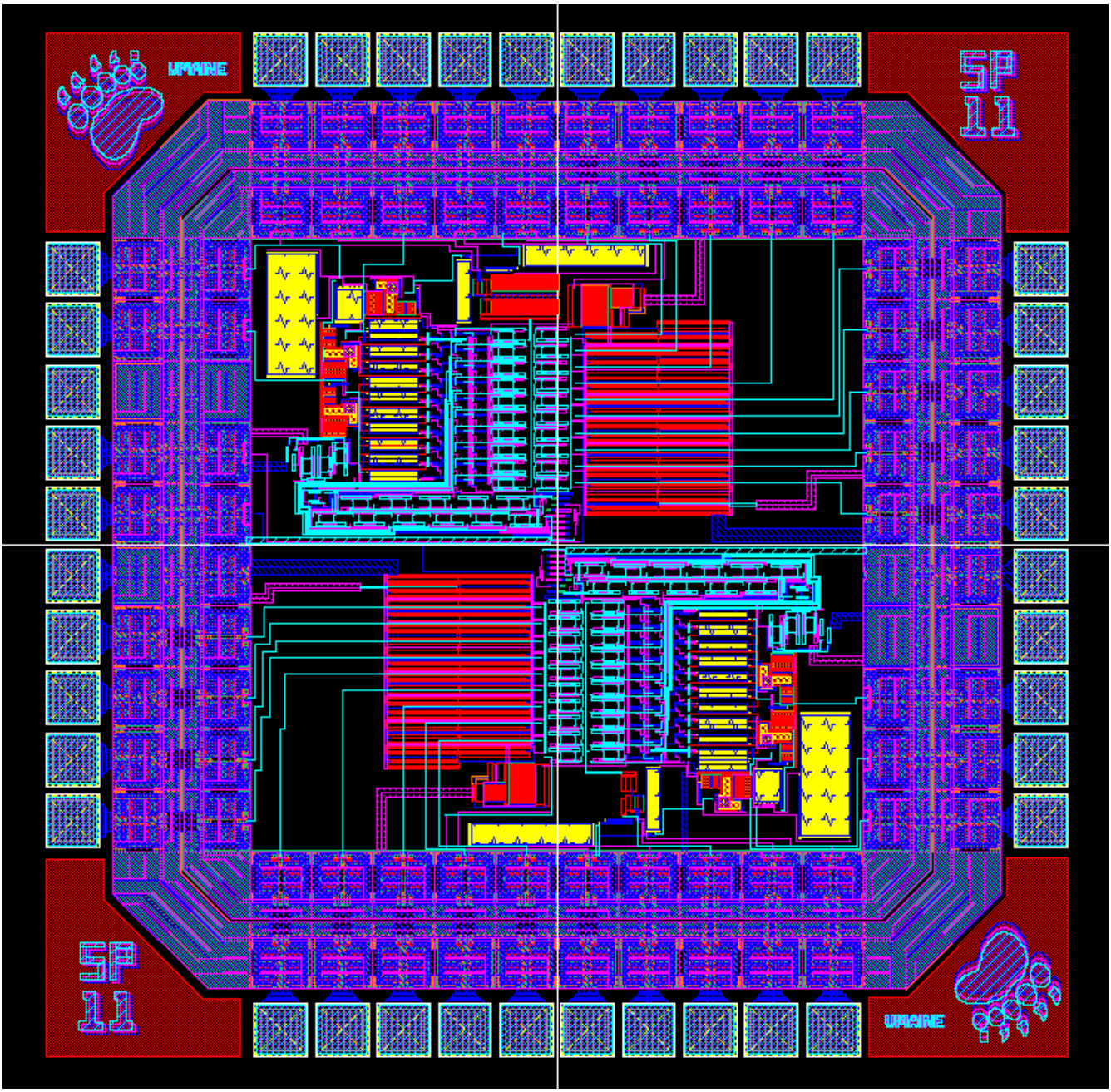

Figure 25: Complete Circuit Layout