

**DESIGN OF A 120 dB
PSEUDO-LOGARITHMIC AMPLIFIER
IMPLEMENTED IN THE AMI 0.5 μ m
PROCESS**

ECE 547

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December 16, 2011

Abstract

This paper discusses the layout, design and simulation of a 120 dB pseudo-logarithmic amplifier. The logarithmic amplifier consists of two major components (1) a series of current limiting amplifiers and (2) a difference amplifier. In this design seven current amplifiers were implemented. The current limiting amplifier (1st one in the series) receives a single ended current input in this design from (1 nA to 1 mA) and produces a single ended voltage which is linear in dB with the input current. The input dynamic range of the pseudo amplifier therefore is 120dB, the rail to rail voltage is 5 VDC and the output voltage range is from 0V to 4V.

The layout of the current amplifier is based on centroid system. Each current amplifier was tested individually in both schematic and in the physical layer and the output voltage was verified. Then all seven of the current limiting amplifiers were connected together and the output was verified. Finally, the difference amplifier was added to the current amplifiers and then the output voltage was verified. The final chip has seven test pins to aid the testing and characterization of the chip.

The difference amplifier is of two stages with a with open loop gain of 80 dB.

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Chapter 1

Introduction

A logarithmic amplifier is an amplifier which provides the logarithmic function.

Linear amplifiers produce an output which is equal to the equation $y=kx$, where y is the output, x is the input, and k is a constant. If the amp is unity-gain, $y=x$ because $k=1$. If the amplifier linearly increases the input signal, k will be greater than 1. If the amplifier reduces the input signal, but retains the linear relationship, k will be less than 1.

A logarithmic amplifier (log amp) produces an output with relation to the input of the logarithmic function. The equation would be $y=K\text{Log}(x)$. The base of the logarithmic function used is usually e , so the equation could be written $y=K\ln(x)$. Again, K is a multiplying constant which scales the output. e^y uses e (the "natural number", about 2.71828) and raises it to the y power. $y=\ln(x)$ means that y is the exponent necessary to get e raised to y equal to x .

An op-amp which is configured as a log-base-10 amp with an output maximum of 5 volts and positive-only input maximum of 1 volt and scaled for 1volt-per-decade will produce:

5volts for 1volt input 4volts for .1volt input 3volts for .01volt input 2volts for .001volt input 1volt for .0001volt input 0volts for .00001volt input

To understand this, look at the inputs for 1 volt and 5 volts output, and compare: for inputs, .0001 volt to 1 volt is a dynamic range of 10,000: the largest value is 10,000 times larger than the input. for outputs, 1 volt to 5 volts is 4 volts, so the largest value is 5 times larger than the input.

The amp could be configured the other way, providing 1 volt for an input of 5 volts, and .00001 volt for an input of 0 volts, with the function being log-base-10. This is an expander, making a small dynamic range into a large one.

Specification	Type/Constraint	Minimum	Maximum
System Input	Single-ended-Current	1nA	1mA
System Output	Single-ended-Voltage	0V	4V
Layout Area	–	$900\mu m \times 900\mu m$	–
Operational Frequency	DC	–	10Hz
Logarithmic Amplification	CMOS only	–	–

Table 1.1: Project Specifications.

1.1 Paper Organization

This report is structured to provide some background on logarithmic amplification, followed by the method of achieving amplification in MOSFET's, followed by circuit designs, and layout techniques used to realize the 120 dB pseudo logarithmic amplifier. Then it describes simulation methodologies and the results of overall system simulation. Chapter 2 Pseudo-logarithmic Approximation: Equation determining the number of stages for the current limiting amplifier, the gain for each stage, I_{out} and I_{sum} . The chapter also explains the Input and the I_{out} current. Chapter 3 Simulation and Matlab results for Number of stages calculation, power and Output current. Chapter 4 Describes the circuit design, layout, testing of the current amplifiers, and op-amp. This section also explain the final system circuit, layout and test. Chapter 5 This chapter describes the manufactured chip test and verification.

1.2 Project Goal and Specifications

The goal of the project is to design a logarithmic amplifier in AMI 0.5um process. This design is implemented only for room temperature at 27 degrees. The specification are shown in the Table 1.1.

Chapter 2

Method Of Achieving Logarithmic Amplification in MOSFET

There are many ways of achieving logarithmic amplification. In this design logarithmic amplification is approximated by summing the outputs of limiting amplifiers. Since in MOSFET devices there are no direct correlation among log function and device characteristics, this approximation method is used.

2.1 Pseudo-logarithmic Approximation

A seven stage cascaded current limiting is used in this design. The details for calculating the gain(G) of the limiting amplifier is explained in section 2.2.1. For this design the number of stages (N) equals seven. The input current I_{in} goes to the first amplifier. The output current I_{out} , from the first stage is connected to the input of the second stage. The general idea is depicted in the figure below.

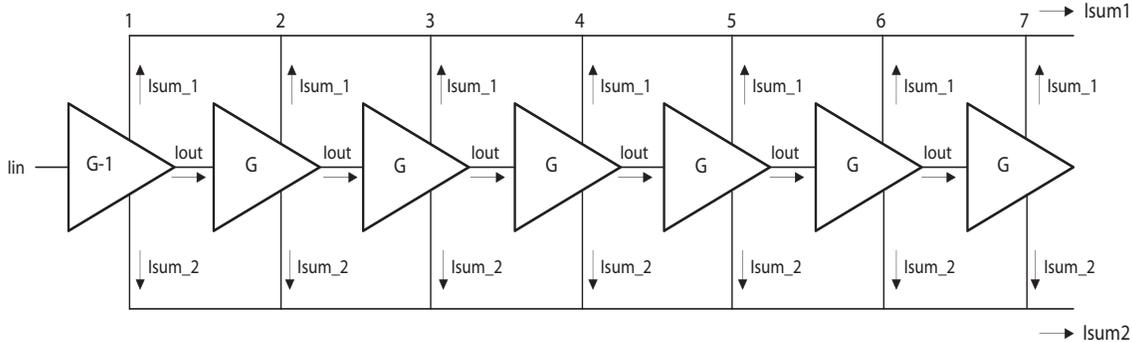


Figure 2.1: Cascaded Configuration of Current Limiting Amplifier

In this circuit topology, the output of each stage is connected to the input of the next stage. The output current of the last stage is not used. Each stage also has two outputs namely I_{sum_1} , and I_{sum_2} . All the I_{sum_1} are added to get I_{sum} and all the I_{sum_2} are added to get I_{sum2} . The following equations are showing the results:

$$I_{sum1} = \sum_{N=1}^7 I_{sum_1} \quad (2.1)$$

$$I_{sum2} = \sum_{N=1}^7 I_{sum_2} \quad (2.2)$$

I_{sum1} and I_{sum2} is then added to the inputs of a difference amplifier. The difference from each stage of I_{sum_1} and I_{sum_2} is added and provides the final result of pseudo logarithmic current. The major aspect of the design is the current is limited from the each limiting amplifier. That means no matter how much the input current may be, the output current stays limited. The maximum output current from each of the limiting amplifier is 1mA regardless of the input current. This feature along with the gain configuration of the cascaded design implements the logarithmic output.

2.2 G, N, I_{in} , I_{out} , I_{sum1} , I_{sum2}

The gain(G), the currents in the design of the limiting amplifier is discussed in the following sections.

2.2.1 Gain and Number of Stages

As shown in figure 2.1 the gain, G for this design has been set to 10; refer chapter 3 for details. The dynamic input range(DIR) for this amplifiers is 120 dB. From the voltage gain standpoint we can write the following:

$$120dB = 20 \log(V_o/V_i)$$

$$(V_o/V_i) = 10^6$$

The input current has the range from 1nA to 1mA giving the 120 dB dynamic range. The gain (G) of the current limiting amplifier is defined by the following equation:

$$G_{cascade} = (G)^{(N-1)} = 10^6 \quad (2.3)$$

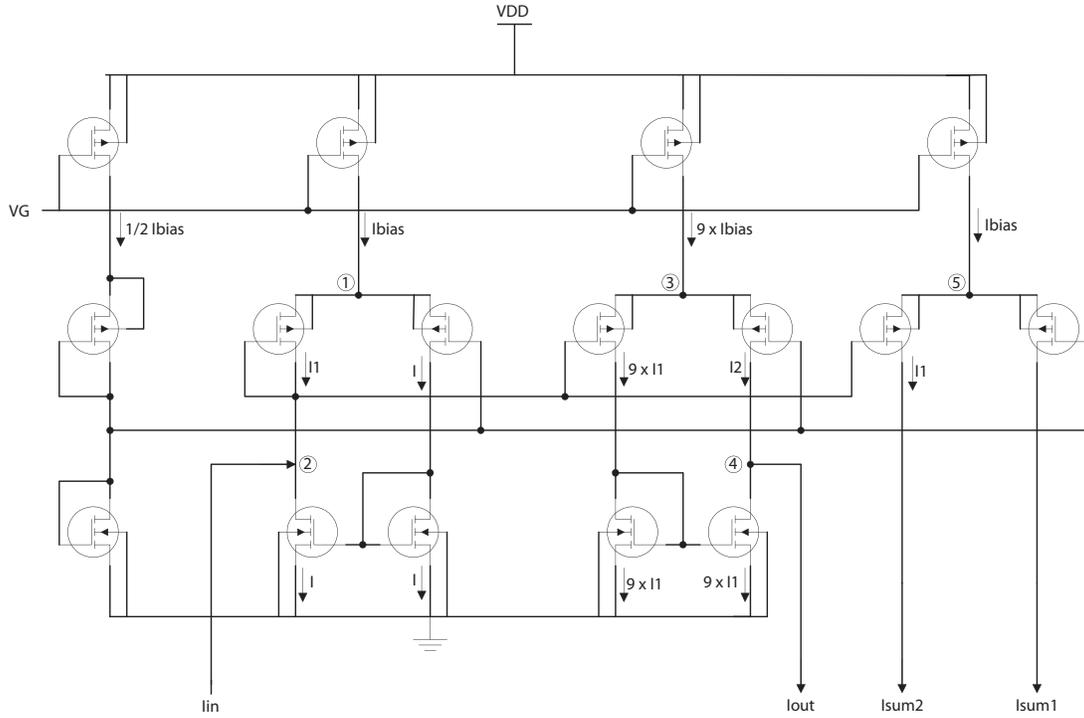


Figure 2.2: Circuit Diagram Current Limiting Amplifiers.

The gain(G) for this design is calculated as:

$$\text{number of stage } N = 7$$

$$G^{(7-1)} = 10^6$$

$$\text{gain of the current amplifier } G = 10$$

The number of stages (N) solely depends on the designer. A 11 stage pseudo amplifier will be designed for my thesis in $180\mu\text{m}$ technology.

2.2.2 I_{in} , I_{out} , I_{sum1} , I_{sum2}

As mentioned in section 2.1, the output current(I_{out}) of the cascade exhibits a linear relationship with the input current (I_{in}) as long the input current is within the range of 1nA to 1mA . We will now find the relationship between I_{in} , I_{out} , I_{sum1} and I_{sum2} through circuit analysis. The reference circuit that is used in this design is from IEEE 1997 Custom Integrated Circuit Conference. We will refer to the figure 2.2 for the circuit analysis. Looking at node 1, we write the following current equation

$$I_{bias} = I_1 + I \tag{2.4}$$

Looking at node 2, we write the following current mirror equation

$$I = I_{in} + I_1 \quad (2.5)$$

$$\Rightarrow I_1 = \frac{I_{bias} - I_{in}}{2}$$

At node 3, the gain is applied. The mirror nodal equation is:

$$9I_{bias} = 9I_1 + I_2 \quad (2.6)$$

$$\Rightarrow I_2 = 9I_{bias} - \frac{9}{2}I_{bias} + \frac{9}{2}I_{in}$$

Looking at node 4, we write the following current mirror equation

$$I_2 = 9I_1 + I_{out} \quad (2.7)$$

$$\Rightarrow I_{out} = 9I_{bias} - \frac{9}{2}I_{bias} + \frac{9}{2}I_{in} + \frac{9}{2}I_{in} - \frac{9}{2}I_{bias}$$

$$\Rightarrow I_{out} = \frac{18I_{bias} - 9I_{bias} - 9I_{bias} + 9I_{in} + 9I_{in}}{2}$$

Therefore, we can write the following relationship between I_{out} and I_{in} for the first stage:

$$I_{out} = 9I_{in} \quad (2.8)$$

Looking at node 5, we write the following current equation for I_{sum1} and I_{sum2}

$$I_{bias} = I_{sum_1} + I_{sum_2} \quad (2.9)$$

but, $I_{sum_2} = I_1$ current mirror

$$I_{sum_2} = \frac{I_{bias} - I_{in}}{2} \quad (2.10)$$

$$\Rightarrow I_{sum_1} = I_{bias} - \frac{I_{bias} - I_{in}}{2}$$

$$I_{sum_1} = \frac{I_{bias} + I_{in}}{2} \quad (2.11)$$

One of the major restriction to this design is that:

$$I_{in} \leq I_{bias} \quad (2.12)$$

I_{sum1} and I_{sum2} from figure 2.1 are connected to the inputs of a difference amplifier. The output the difference amplifier depicts the log current I_{LOG} which is expressed in the following equation:

$$I_{LOG} = I_{sum2} - I_{sum1} \quad (2.13)$$

Stage	Iin(nA)	Iout(nA)	Isum_2(mA)	Isum_1(mA)	I _{LOG} (mA)
1	1	9	0.4999995	0.5000005	0.000001
2	9	90	0.499995	0.500005	0.0000095
3	90	900	0.49995	0.50005	0.000095
4	900	9000	0.49955	0.50045	0.00095
5	9000	90000	0.4955	0.5045	0.009
6	90000	900000	0.455	0.545	0.09
7	900000	9000000	0.05	0.95	0.9
-	-	-	-	Σ	1.000055 \approx 1

Table 2.1: Current Calculations for Seven Stage Cascade, Iin=1nA

2.2.3 Calculating Iout, Isum1, Isum2 and I_{LOG}

As stated in subsection 2.2.1, the DIR for this amplifier is set from 1nA to 1mA. We will now calculate the Iout, Isum1, Isum2 and I_{LOG} in the following tables. These current values are calculated using equation 2.8, equation 2.10, equation 2.11 and equation 2.13. The bias current is:

$$I_{bias} = 1mA$$

The table 2.1 is for input current Iin = 1nA, which is the minimum leftmost value for DIR. Table 2.2 is for input current Iin = 10nA Table 2.3, Iin equals 1mA, which is the maximum rightmost value for the DIR. Beyond this value the linearity of the amplifier ceases and the I_{LOG} saturates to its maximum of 7mA. We will see in the following, when $I_{in} \geq 1$ mA, Iout limits to 9mA for first stage and 10mA for the consecutive stages. For Iin1mA,

$$I_{sum_2} = 0; \quad I_{sum_1} = 1$$

Stage	I _{in} (nA)	I _{out} (nA)	I _{sum_2} (mA)	I _{sum_1} (mA)	I _{LOG} (mA)
1	10	90	0.499995	0.500005	0.00001
2	90	900	0.49995	0.50005	0.00009
3	900	9000	0.49955	0.50045	0.0009
4	9000	90000	0.4955	0.5045	0.009
5	90000	900000	0.455	0.545	0.09
6	900000	9000000	0.05	0.95	0.9
7	9000000	9000000	0.05	0.95	0.9
-	-	-	-	Σ	1.9 \approx 2

Table 2.2: Current Calculations for Seven Stage Cascade, I_{in}=10nA

Stage	I _{in} (mA)	I _{out} (mA)	I _{sum_2} (mA)	I _{sum_1} (mA)	I _{LOG} (mA)
1	1	9	0	1	1
2	9	10	0	1	1
3	10	10	0	1	1
4	10	10	0	1	1
5	10	10	0	1	1
6	10	10	0	1	1
7	10	10	0	1	1
-	-	-	-	Σ	7

Table 2.3: Current Calculations for Seven Stage Cascade, I_{in}=1mA

Chapter 3

Matlab Implementation

The current amplifier amplifier design is verified through Matlab model via Simulink. Then the number of stages (N) was determined based on the lowest power consumption. These are presented in the following sections:

3.1 Simulink Simulation

The simulink model in figure 3.1 replicates the seven stage pseudo cascaded current limiting amplifier design. This model is similar to the one created by [1] in his report on designing pseudo logarithmic amplifier. This model is modified for this design. This figure is similar to figure 2.1. In this diagram, each current amplifier is represented by the "Product" block. The Gain (G) for the 1st amplifier is represented by the "Constant1" block which has a gain of 9, and the gain for the following stages are represented by the block "Constant" which has a gain of 10. Each of the block represented by "Saturation" has a minimum value of 0 and maximum value of 1000000 representing the DIR of 120 dB. The summation of all the seven "Saturation" blocks, provides the total I_{LOG} current. The figure 3.2 shows the linearity of the I_{LOG} current. The x axis represents the DIR from 0 to 10^6 and the y axis represents the log current I_{LOG} . For example, at 10nA, the total I_{LOG} is 2mA, and at 1mA input the total I_{LOG} is 7mA . The plot verifies the table 2.3, where the we see that after the seven stages the total I_{LOG} is 7mA.

3.2 Power Versus Number of Stages

From the power equation below:

$$P = V * I_{CASCADE} \quad (3.1)$$

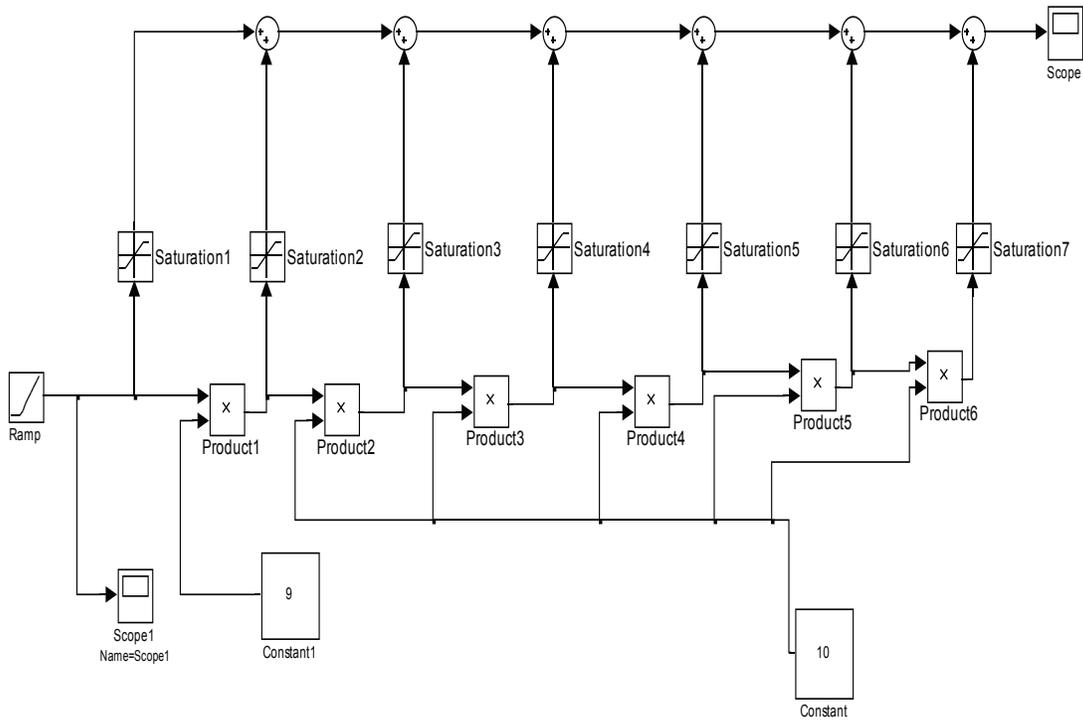


Figure 3.1: 7 stages Pseudo Logarithmic model in Simulink

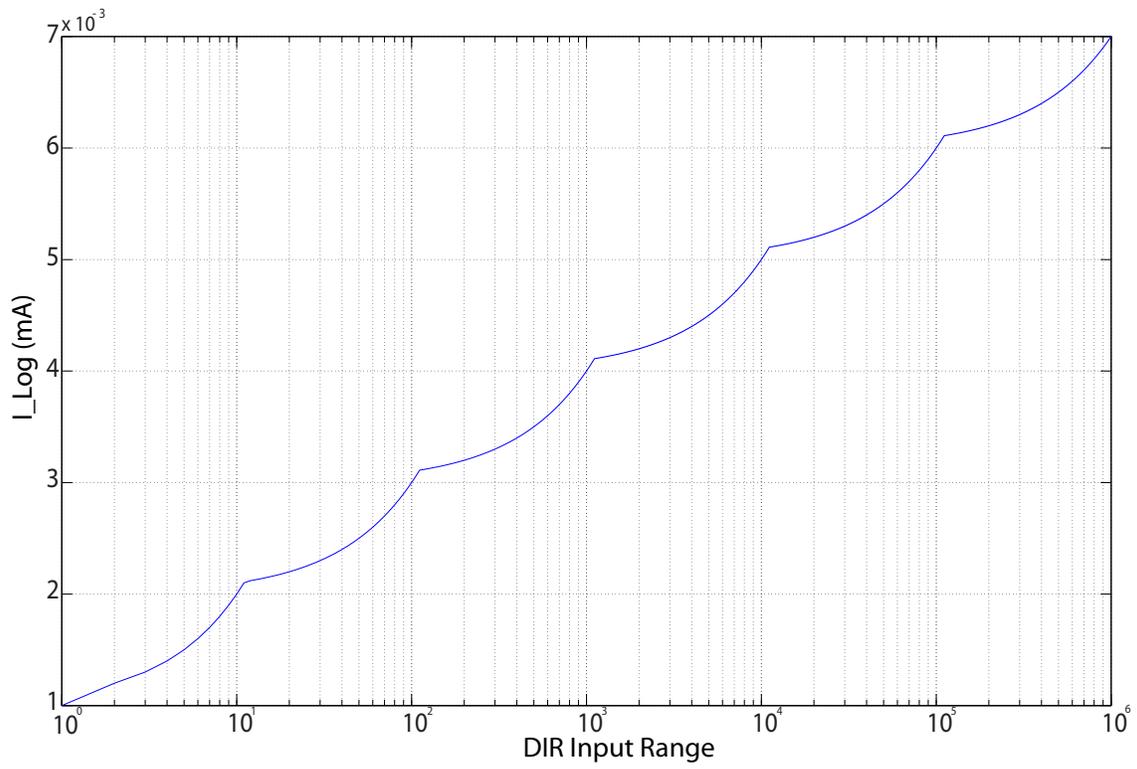


Figure 3.2: Output of the seven stage limiting amplifier

we can derive an equation that relates power to the number of stages (N). We will refer to the figure 2.2 to calculate $i_{cascade}$. As we know that the gain (G) in the 1st stage is (G -1) and the gain onwards is only calculated as G. So looking at the schematic we can derive the following: The total current in the 1st stage can be written as:

$$I_{1st\ stage} = (1/2)I_{bias} + I_{bias} + (G - 1)I_{bias} + I_{bias} \quad (3.2)$$

from here we can derive the following:

$$I_{1st\ stage} = 2.5I_{bias} + I_{bias} * (G - 1) \quad (3.3)$$

The total current in the 2nd stage, can be written as:

$$I_{2nd\ stage} = 2.5I_{bias} + G * I_{bias} \quad (3.4)$$

from here we can derive the following:

$$I_{2nd\ stage} = (1/2)I_{bias} + I_{bias} + G * I_{bias} + I_{bias} \quad (3.5)$$

Therefore total current for all the stages will be adding 1st and 2nd stage so:

$$I_{CASCADE} = [2.5I_{bias} + I_{bias}(G - 1) + (N - 1)(2.5I_{bias} + G * I_{bias})] \quad (3.6)$$

We write power as

$$P = V * I_{CASCADE}$$

where,

$$V = 5.0volts$$

Therefore, power can be written as:

$$P = 5 * [2.5 * I_{bias} + I_{bias}(G - 1) + (N - 1)(2.5 * I_{bias} + GI)] \quad (3.7)$$

we know that gain G equals:

$$G^{N-1} = 10^6$$

or,

$$G = \sqrt[N-1]{10^6}$$

here,

$$I_{bias} = 1mA$$

Now substituting the values of G and I_{bias} in equation 3.7 and using Matlab, we get the figures 3.3. From this figure we can say that stages N = 7 is close to the lowest power but N = 11 would be the lowest power consumption for the limiting amplifiers. The first derivative of equation 3.7 is plotted in figure 3.4. This plot intersects "0" power at N=10 but not at N=7. So, this design the power consumption will not be the lowest.

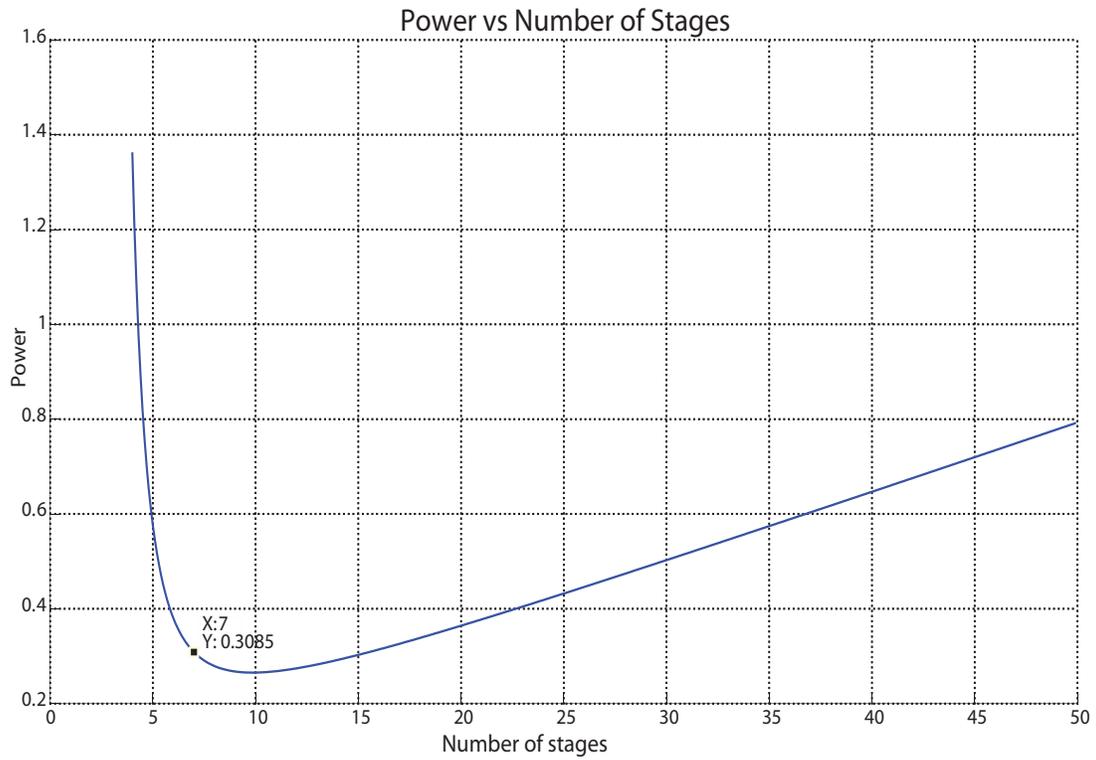


Figure 3.3: Number of Stages and Corresponding Power

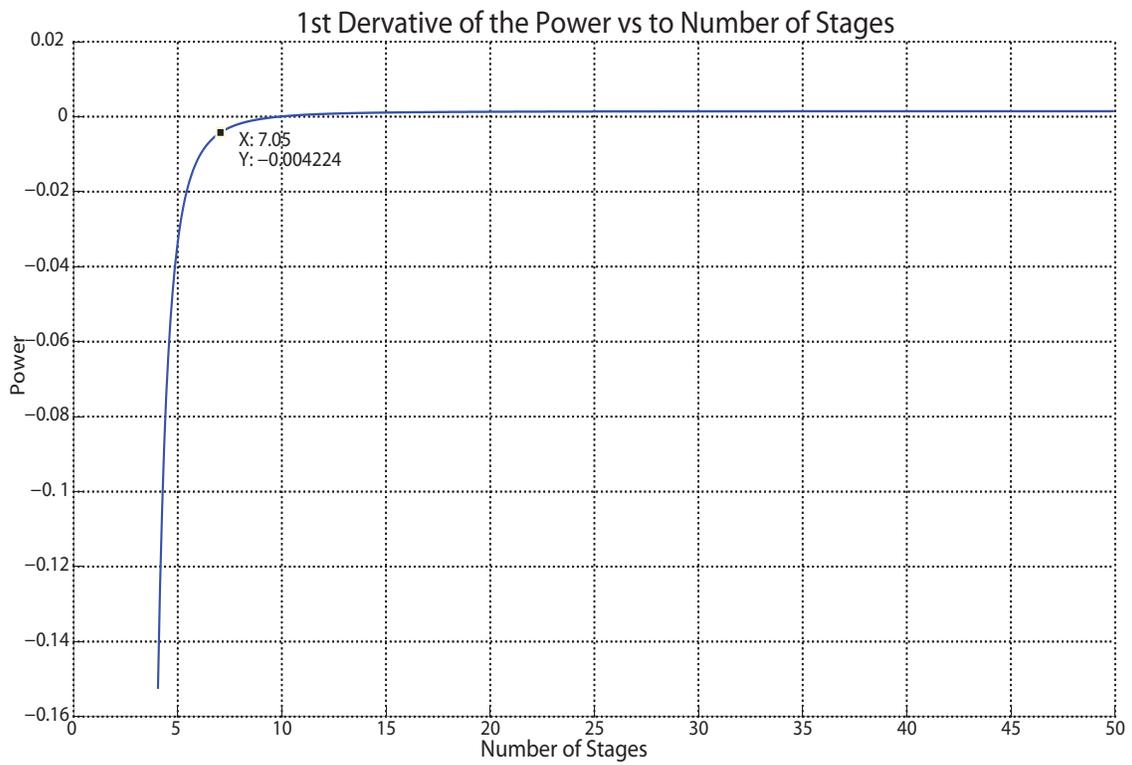


Figure 3.4: 1st Derivative Number of Stages versus Power

Chapter 4

Design of the Pseudo Logarithmic Amplifier

The circuit of this design is taken from the IEEE 1997 Custom Integrated Circuits Conference which utilizes a single input and provides the single ended output. The description of the circuit is given in the next section.

4.1 Circuit of the Limiting Amplifier

The figure 4.1, is similar to the reference circuit presented in the IEEE 1997 conference [2]. Looking at the circuit, the 1st leg the PMOS $p13$, is not a mirror connection that of the reference circuit. The ratio of all the W/L are also different than that of the reference circuit. The values of the W/L for PMOS transistor are picked for large devices for $L = 2.4\mu$ with 3 : 1 ratio between width and the length. The values of the W/L for NMOS transistor were chosen based on the biasing and the output characteristics of the limiting amplifier. In the 1st leg, $P5$ diode connected to $N0$ setting the gate voltage for $P7$, $P8$, and $P9$. In the 2nd leg, $P6$, is mirror to $P10$, and $P11$. The lower NMOS connected to GND all gates except for the 1st one are connected to each other. On the 2nd and 3rd leg both NMOS pairs have mirror connections. Subsection 2.2.3 explains how the circuit works and the relation of the various currents to the gain of the design.

4.2 Layout of the Limiting Amplifier

There are two major design aspects of the layout

- Centroid Layout

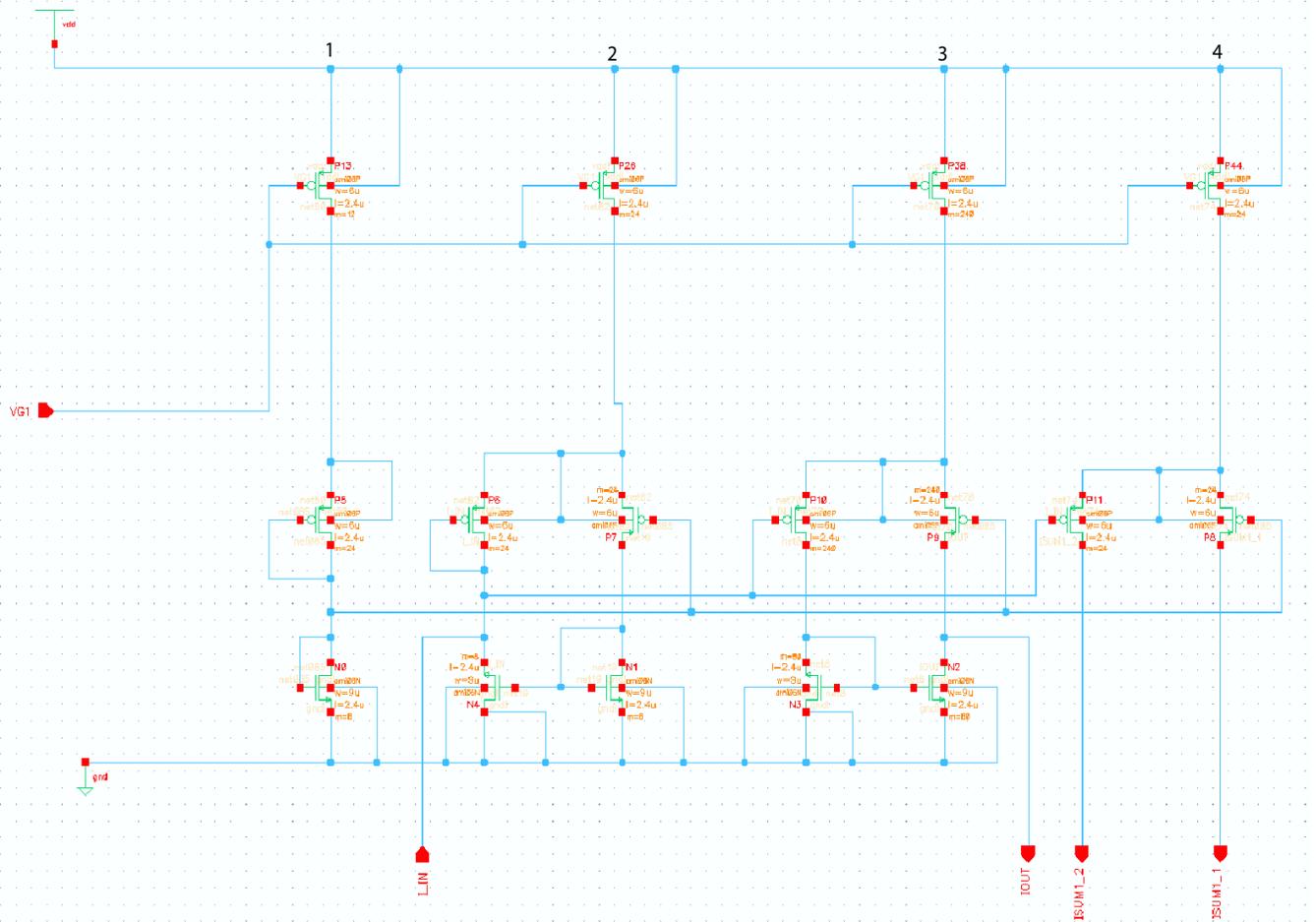


Figure 4.1: 10X Current Limiting Amplifier Circuit

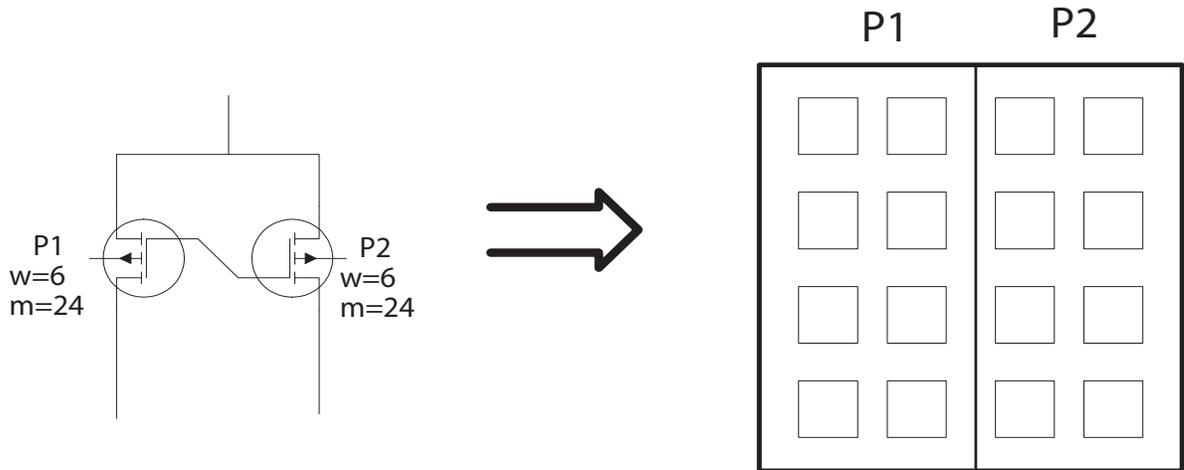


Figure 4.2: Centroid Layout

- Transistor Width

These topics are discussed in the following sections.

4.2.1 Centroid layout

Beside the single PMOS and NMOS transistors all the rest of the paired PMOS and NMOS transistors were designed in the layout by centroid system. In the figure 4.3, we can observe this layout pattern. In centroid layout calculation, each transistor in the pair is assumed to be eight transistors, refer to figure 4.2. A pair will have sixteen transistors as of the following figure: The total width has to be a multiple of 8 while keeping the width of the transistor the same. As a result, the multiplier(m) will be modified that from the schematic. For example the pairs $P9$ & $P10$ and $N4$ & $N1$ from figure 4.1 will be discussed below for the centroid calculation:

$$\text{Schematic : } m \times w = 240 \times 6\mu = 1440\mu$$

$$\text{Layout : } m \times w = 8 \times 9\mu = 9\mu \times 8 = 1440\mu$$

and for $N4$ & $N1$

$$\text{Schematic : } m \times w = 8 \times 9\mu = 72\mu$$

$$\text{Layout : } m \times w = 1 \times 9\mu = 9\mu \times 8 = 72\mu$$

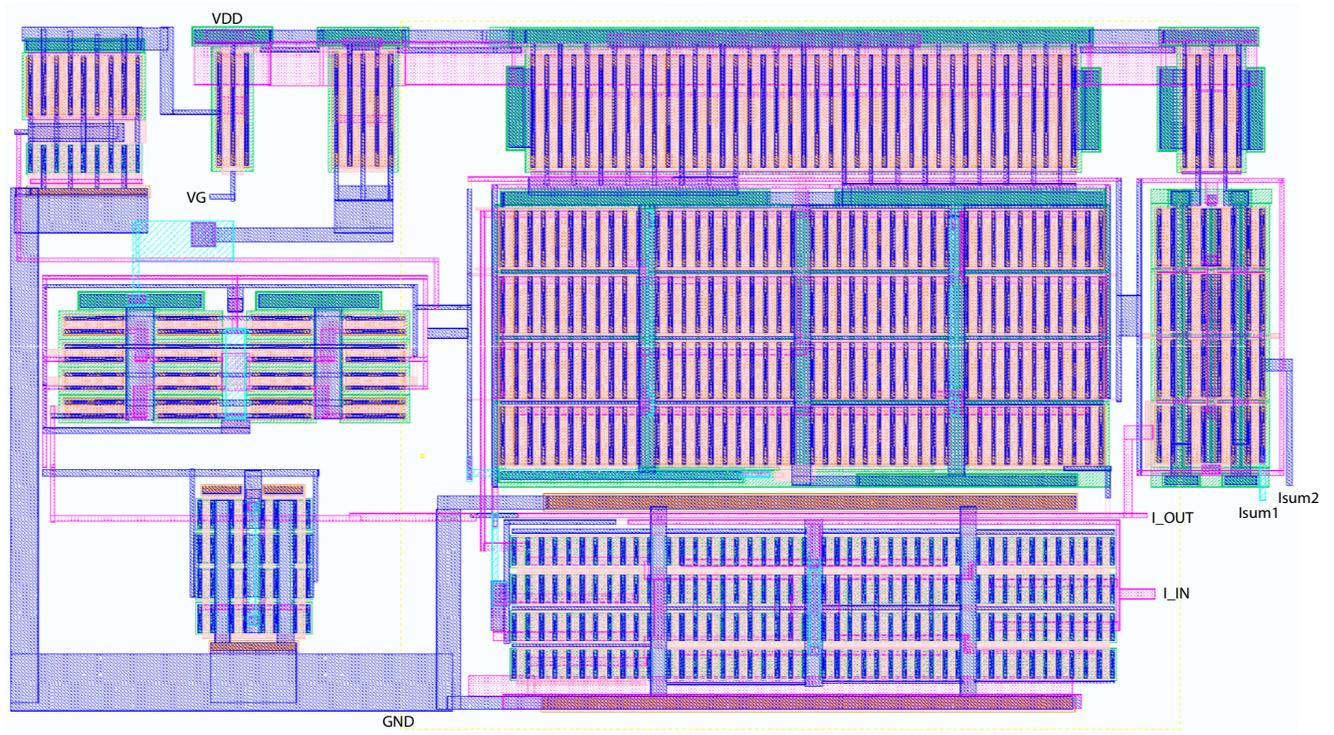


Figure 4.3: 10X Current Limiting Amplifier Layout

4.2.2 Figuring the Width into Layout

According to Gray's book [3] The effective channel width of an MOS transistor is determined by the gate dimension parallel to the surface and perpendicular to the channel length over which the gate oxide is thin. The width of a nitrate region corresponds to the drawn width of a transistor. Both the effective lengths and the effective widths of transistors differ from the corresponding drawn dimension. In analog design, the change in the effective length is usually much more important than the change in the effective width because transistors usually have drawn lengths much less than their drawn widths. As a result, the difference between the drawn and effective width is often ignored.

With this conception in mind I made the initial layout where in the 1st, 2nd row's the PMOS in figure 4.3 the width were different although the total width for each individual PMOS would be same that from the schematic similar to in figure 4.1. I had the similar case for the NMOS; the width's of the NMOS transistor differ from each other although the total width remains the same. The design passes LVS; but when tested to validate the design, the output plot are very varies substantially between the schematic and the layout. It seems that in the layout there is more current in the 1st stage of the cascaded amplifier than it supposed to be!

Lots a speculation and test were performed to understand and overcome this issue. It was until I saw the following effective width equation on the [4] BSIM3v3 Manual. The effective channel length and width used in all model expressions is given below:

$$W_{eff} = W_{drawn} - 2dW \quad (4.1)$$

$$W_{eff}^l = W_{drawn} - 2dW^l \quad (4.2)$$

The only difference between equation 4.1 and equation 4.2 is that the former includes bias dependencies. The parameters dW and dL are modeled by the following:

$$dW = dW^l + dW_g V_{gsteff} + dW_b (\sqrt{\phi - V_{bseff}} - \sqrt{\phi_s}) \quad (4.3)$$

From the equation, it is apparent that the effective and the drawn width that Cadence use is different. Effective width is a function of W(drawn), and their associated product terms from the equation.

Cadence software uses the associated parameters while calculating W(drawn) as well as L(drawn). Since in this design L is the same value so it did not effect the design as it did for W. Therefore while for a column of transistor to work properly, the width has to be same. The multiplier could be of different value but the width has to be the same in order to get the $W_{Effective}$ and W_{drawn} calculated properly.

4.2.3 Testing the Configured Layout

Once the layout was done, a symbol is created in cadence. This symbol represents the physical layout of the single current limiting amplifier. The following test circuit figure 4.4 is created to test the output in terms of voltage. The bias voltage is set to 2.4 volts. The input current I_{IN} is connected to an current source I5 that is connected to V_{dd}. I5 is a variable with the DIR from 1nA to 1mA. The I_{sum1} and I_{sum2} is measured across 1K resistors.

4.2.4 Result of the Configured Layout

From the figure 4.5 we can see that at 1nA the difference between I_{sum1} and I_{sum2} is 977pA \approx 1nA and at 1mA the difference is $I_{sum1} - I_{sum2} = 1.5 - 0.5 = 1mA$

4.3 Subsystem

After achieving the design goal of the single current amplifier, we now move on to the cascaded design phase. The following sections discusses the circuit, layout, test circuit and the test result.

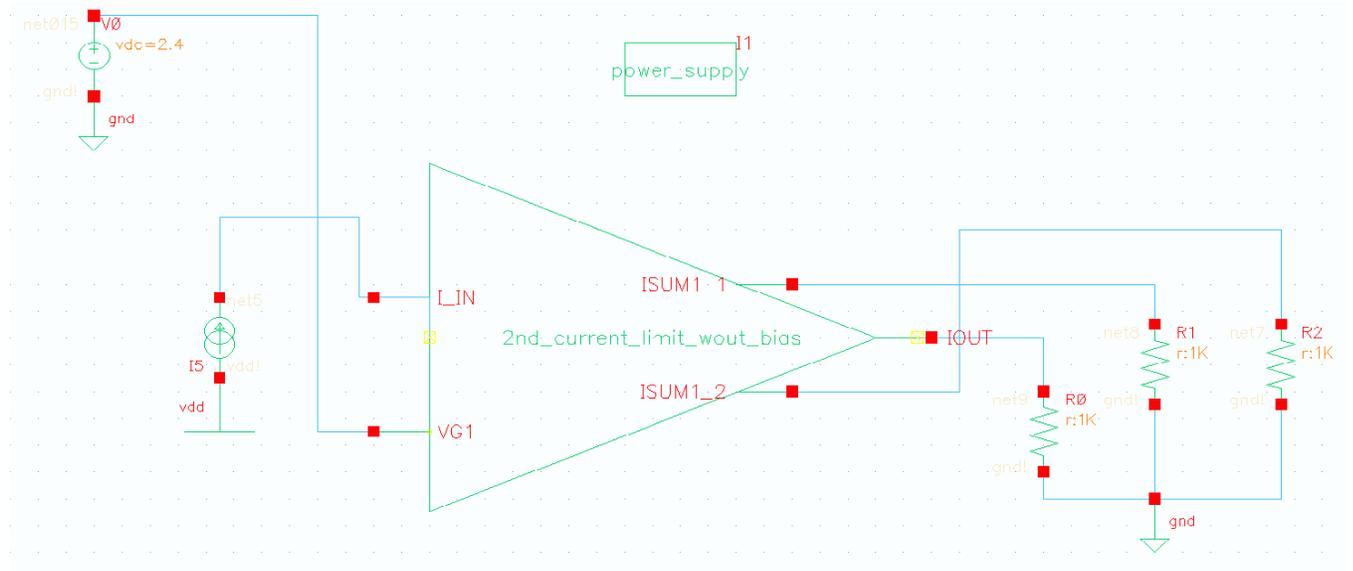


Figure 4.4: Current Limiting Amplifier Test Circuit

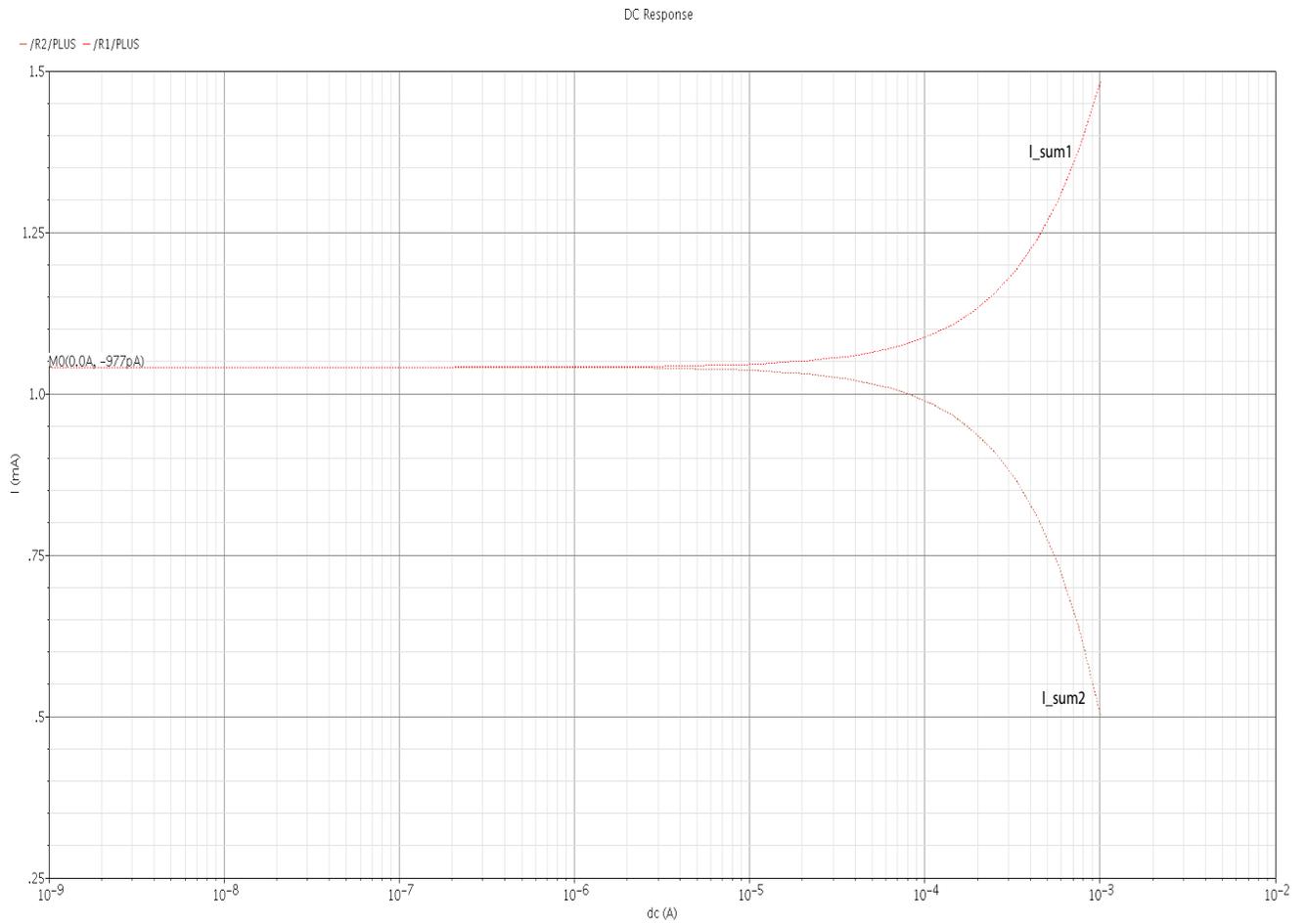


Figure 4.5: Isum1 and Isum2 Difference

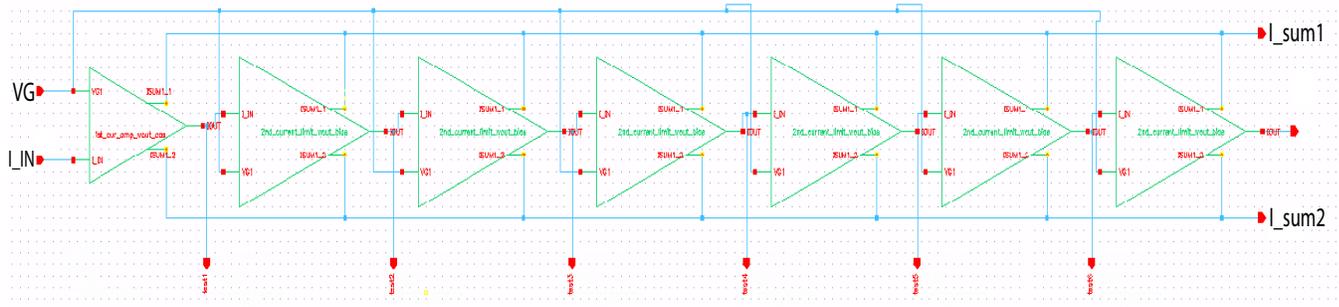


Figure 4.6: Cascaded Current Limiting Amplifiers

4.3.1 7 stage schematic

The 7 stage cascaded circuit configuration is referred to the figure 4.6. This figure is similar to that of figure 2.1 in section 2.1. The reason for adding 7 stages refers to subsection 2.2.1. The 1st stage the gain is 9 and all other stages the gain is 10. All the Isum1 and Isum2 are connected respectively. The Iout of the 1st stage is connected to the Iin of the next stage and so on. In this circuit seven test pins are added to measure the IOU_T after each stage.

4.3.2 7 stage layout

While doing the layout, the main concern was to fit all seven stages inside the chip active area which is $900\mu \times 900\mu$ and have space for the difference amplifier. The vdd and gnd connections are made on the external to the stages and all the internal connections are laid out within the stages. This way it would be easier to connect I.sum2 and I.sum1 to the difference amplifier, and connect the VG, gnd, LIN and L-OUT pins to the pins external to the chip.

4.3.3 7 stage config test

Unlike the testing described in the prior sections, a symbol was created in cadence representing the 7 stage. The figure 4.8 represents the test circuit. This circuit is similar to the test circuit figure 4.4. Only difference is this symbol has the added test pins. The output will be represented in the form of single ended voltage.

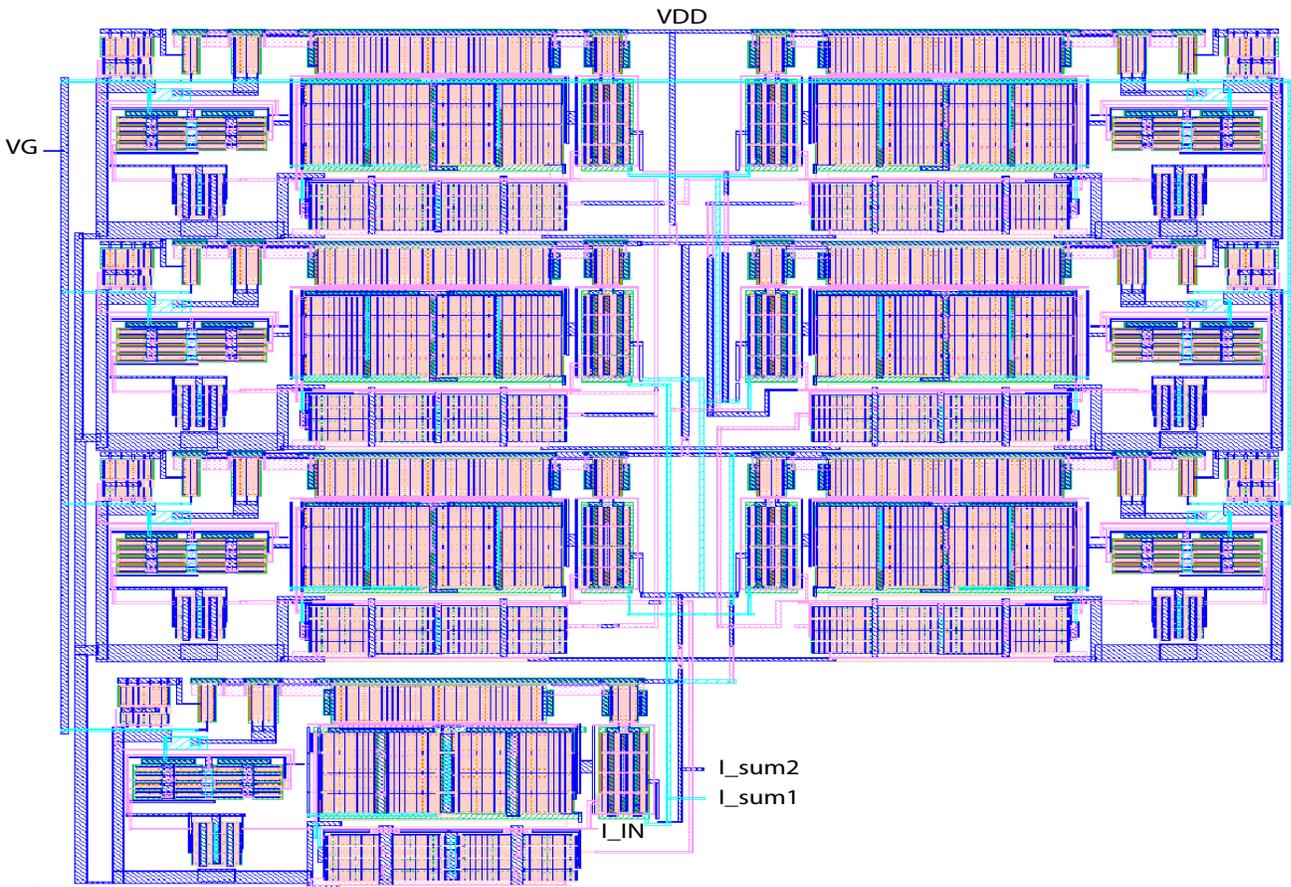


Figure 4.7: 7 Stage Current Amplifier Layout

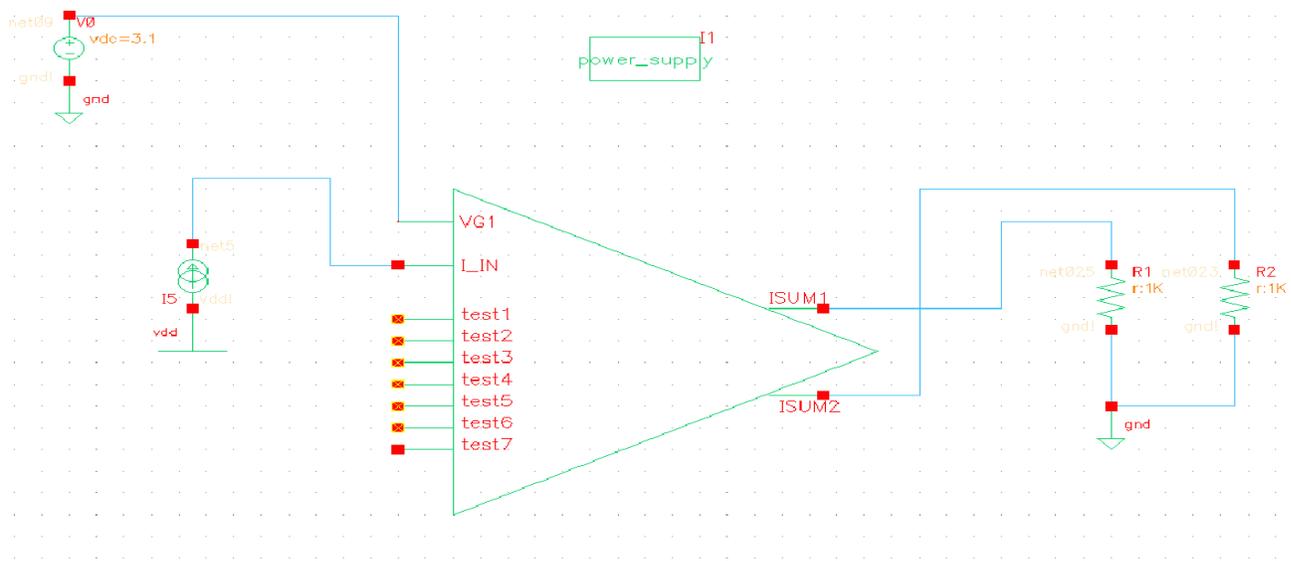


Figure 4.8: 7 Stages Test Circuit

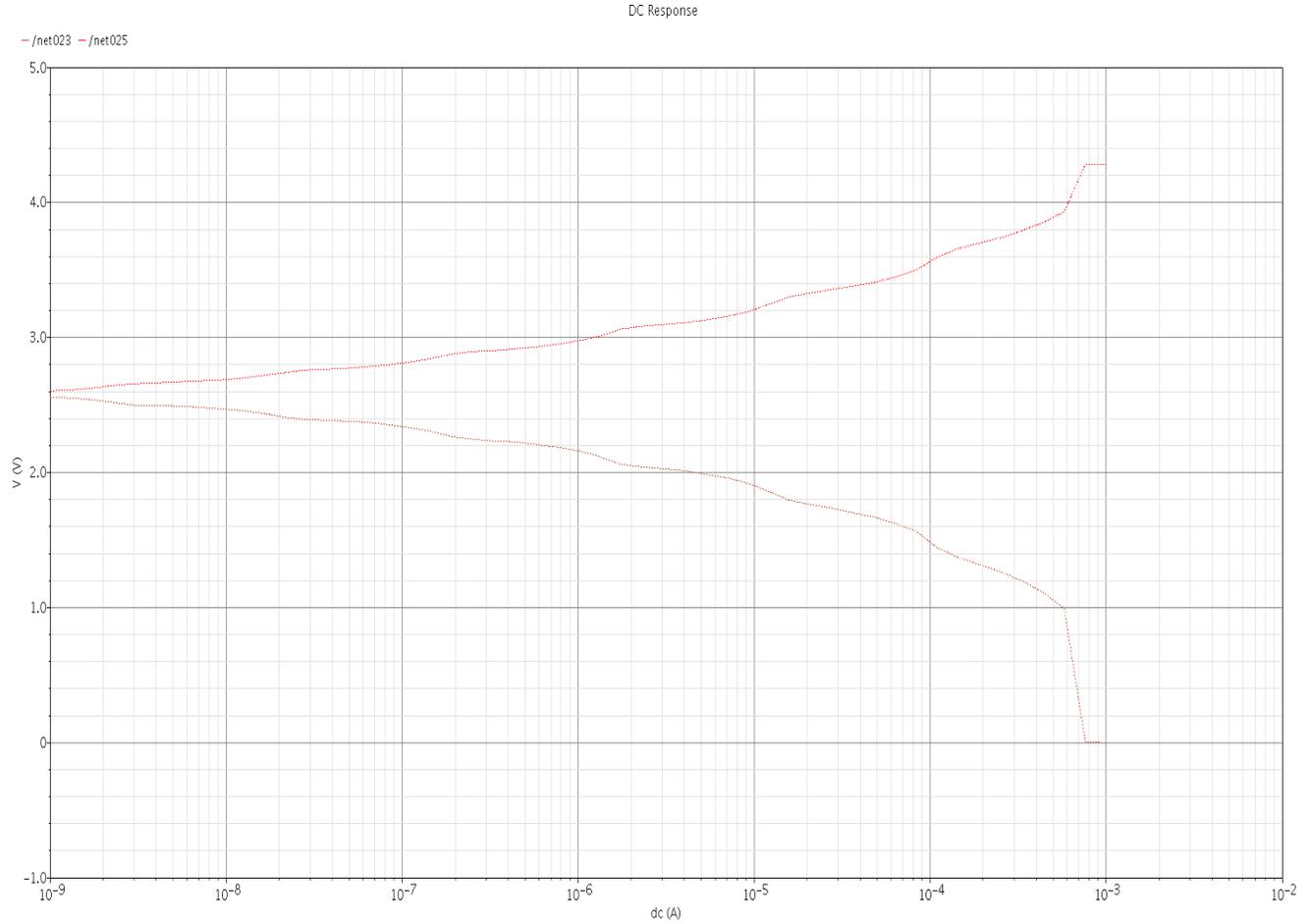


Figure 4.9: 7 Stages Test Plot

4.3.4 7 stage config test results

Looking at the figure 4.9, we see that the stayed very close to within 0 volts to 4 volts which is the specified output voltage range. The DIR is within 120 dB which is also the specified range. The reason both the upper bound and the lower bound lines did not intersect 10^{-3} mark evenly is because the PMOS to NMOS ratio in the original circuit refer to fig 4.1, is not quite perfect.

4.4 Circuit of the Operational Amplifier

As mentioned in the previous sections, the overall design of the pseudo logarithmic amplifiers design has two major components. The cascaded current amplifiers connected with a operational amplifier that is configured as a differential amplifier. The cascaded amplifier takes the single-ended current input I_{in} . The difference amplifier serves two purposes; it

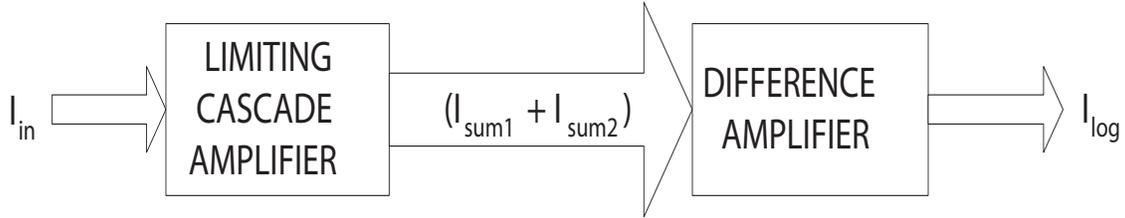


Figure 4.10: Overall Pseudo-Logarithmic Amplifier Architecture

allows the summing outputs from the cascaded amplifiers to be subtracted and produces a single-ended voltage output V_{log} . The figure 4.10 shows the concept. A two stage high swing op-amp is designed for pseudo-logarithmic amplifier. The level shift design implemented for the current mirror, makes the output voltages within 2 times overdrive voltage:

$$V_{OUT(min)} \cong 2V_{ov}$$

By this design, the current amplifier puts less restrictions on the range of output voltages that can be achieved by the op-amp. So, a wider range of output voltage can be selected. The op-amp is sized empirically by simulation and by calculation mentioned in Gray's [3] book. In order to assure sufficient stability and gain to make the difference amplifier functional. For common-source (M5) amplifier there is a trade-off between maximum gain and maximum operating frequency. In this design the maximum gain was considered since the frequency is DC. As a result, the feed back pole is less than the expected 3 dB frequency, therefore a $\cong 10pF$ capacitor is placed from the output to drain of M5 of the Op-Amp. The design was finalized with a flat-band gain of 80 dB, a gain margin of 19 dB and a phase margin of 13 degrees. The bandwidth of the op-amp is of no concern since the overall system will be operating in DC. The power consumption is negligible compared to that of the limiting cascade.

4.4.1 Operational Amplifier Layout

The layout of the op-amp was quite straight forward as shown in figure 4.12. The capacitor took more space than the rest of the elements in the layout. But still leaving plenty of room within the bond-pad ring to layout the cascaded amplifiers.

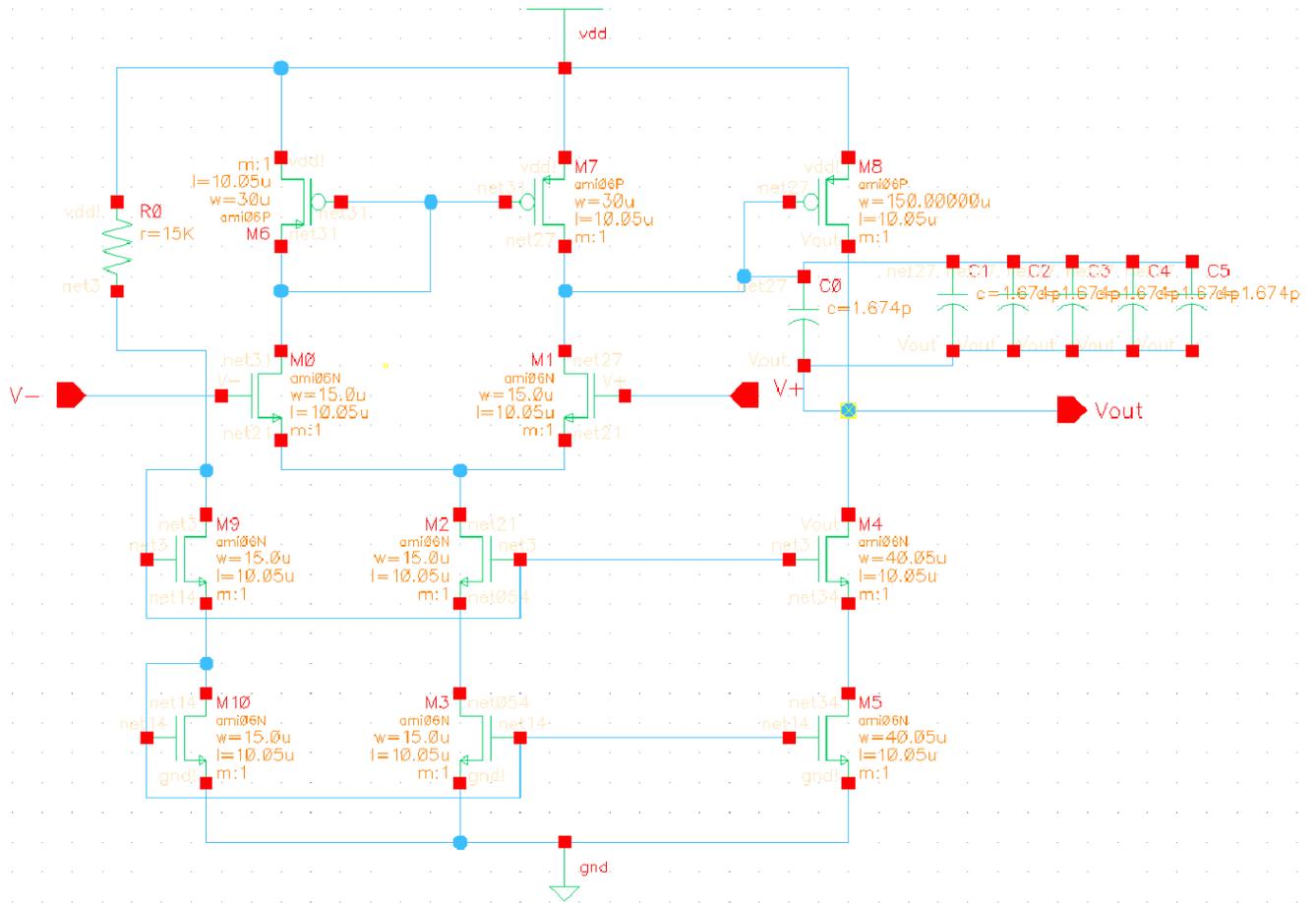


Figure 4.11: High Swing Operational Amplifier

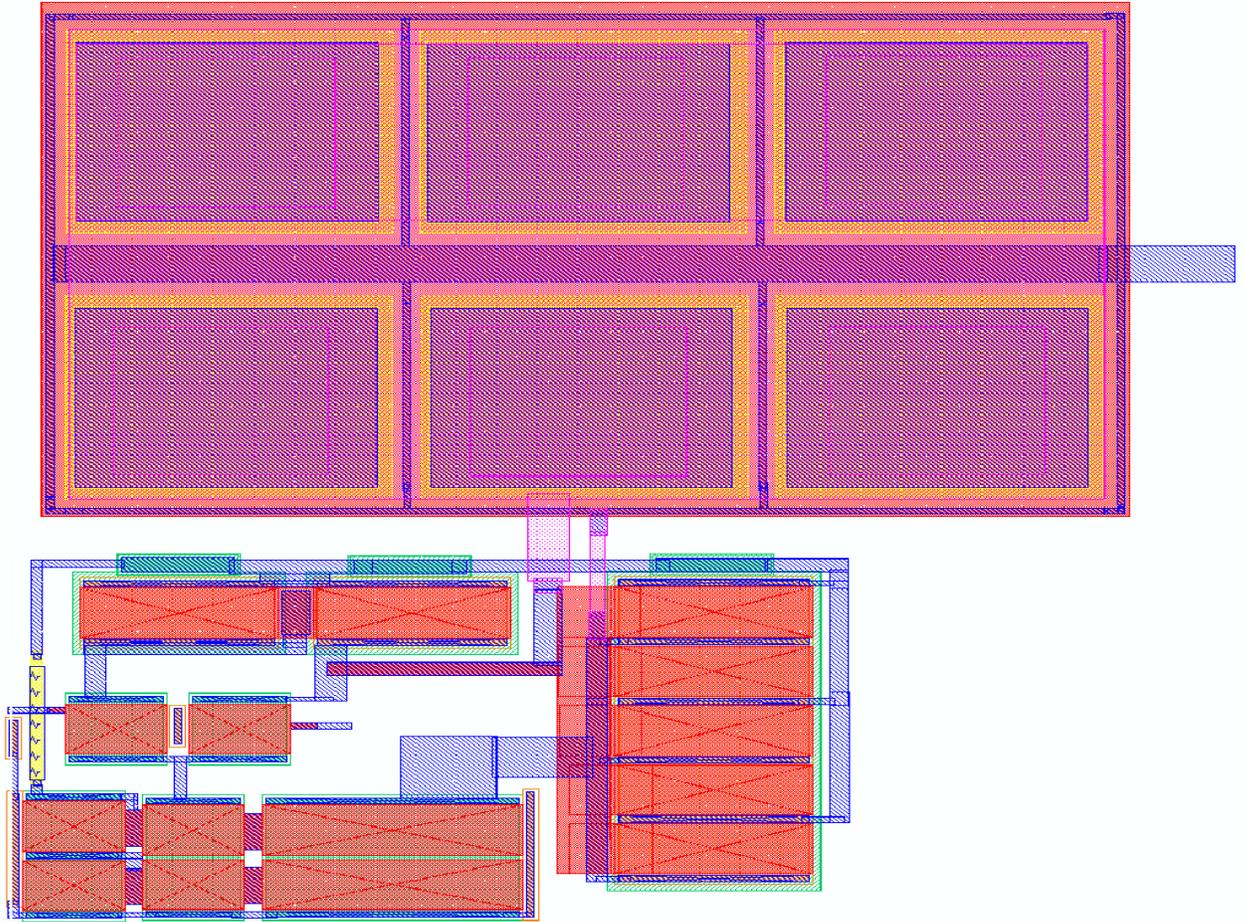


Figure 4.12: Operational Amplifier Layout

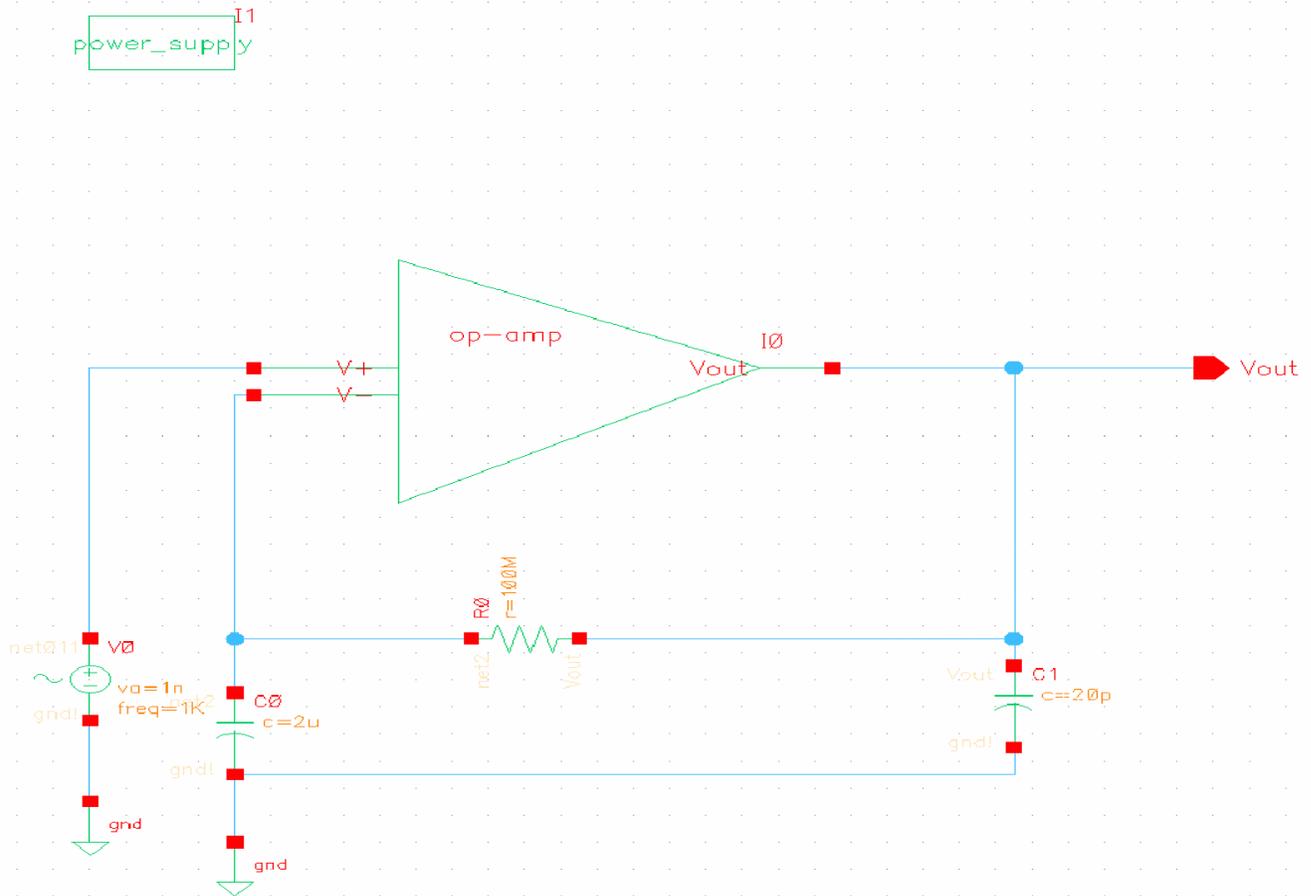


Figure 4.13: Operational Amplifier Test Circuit

4.4.2 Testing the Op-Amp

The op-amp was tested with an ideal AC source for gain margin, stability and phase margin. The test circuit is shown in figure 4.13. It was configured as a non-inverting op-amp for the test purpose. The two capacitors C0 and C1 is used. The capacitor functions to reduce gain at higher frequencies.

4.4.3 Stability of the Op-Amp

From the plot in figure 4.14, we see that the open loop gain is $\cong 83.97dB$ stability is -9.727 and phase margin is $\cong 57$ degrees. For the result we can conclude that the op-amp is stable for the input range.

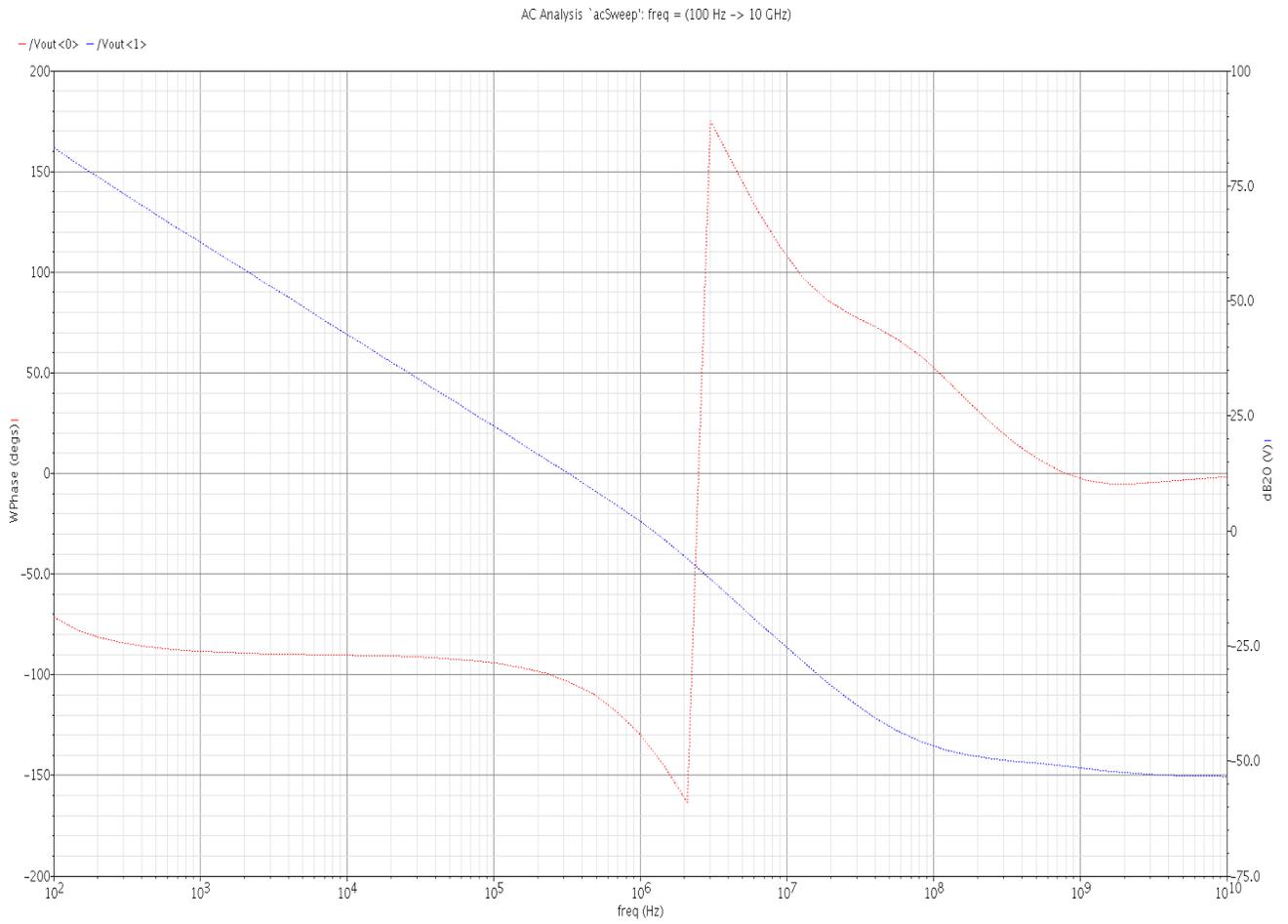


Figure 4.14: Operational Amplifier Output Plot

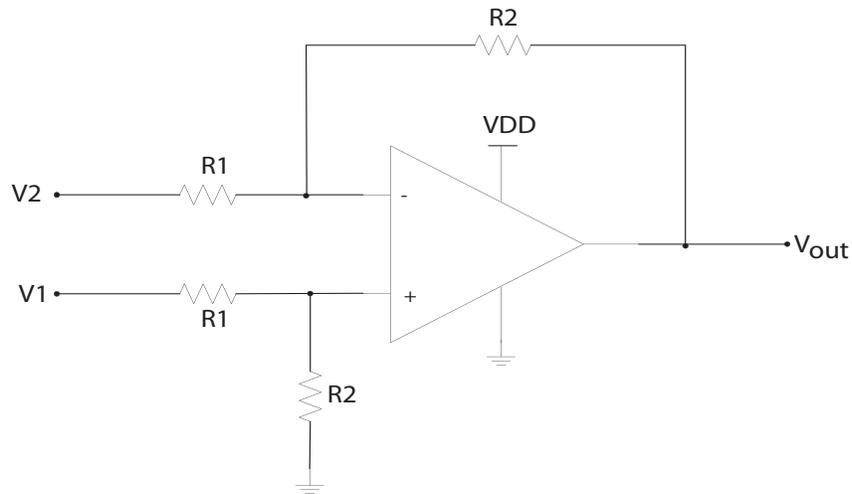


Figure 4.15: Difference Amplifier Configuration

4.4.4 Difference Amplifier

The two stage amplifier described above was then connected into a difference amplifier configuration as shown in the figure 4.15 below. The output voltage of this difference amplifier exhibits the following relationship:

$$V_{out} = \frac{R2}{R1}(V_1 - V_2) \quad (4.4)$$

The two summing currents I_{sum1} and I_{sum2} mentioned in the previous sections, will be connected to R1 and R2 respectively. Thus creating the voltage V2 and V1 at the input for the difference amplifier. The amplifier will then add all the summing currents and will take the difference between Voltages V1 and V2 to provide the final single ended output voltage V_{out} .

4.5 Final System

All the system blocks that were mentioned in the previous sections are now put together to make the final system in the figure 4.16. This figure is similar to the figure 4.10. The first part is the cascaded limiting amplifier and the second part is the op-amp configured as a difference amplifier. Unlike the previous sections this final system has a the following sub sections detailed below:

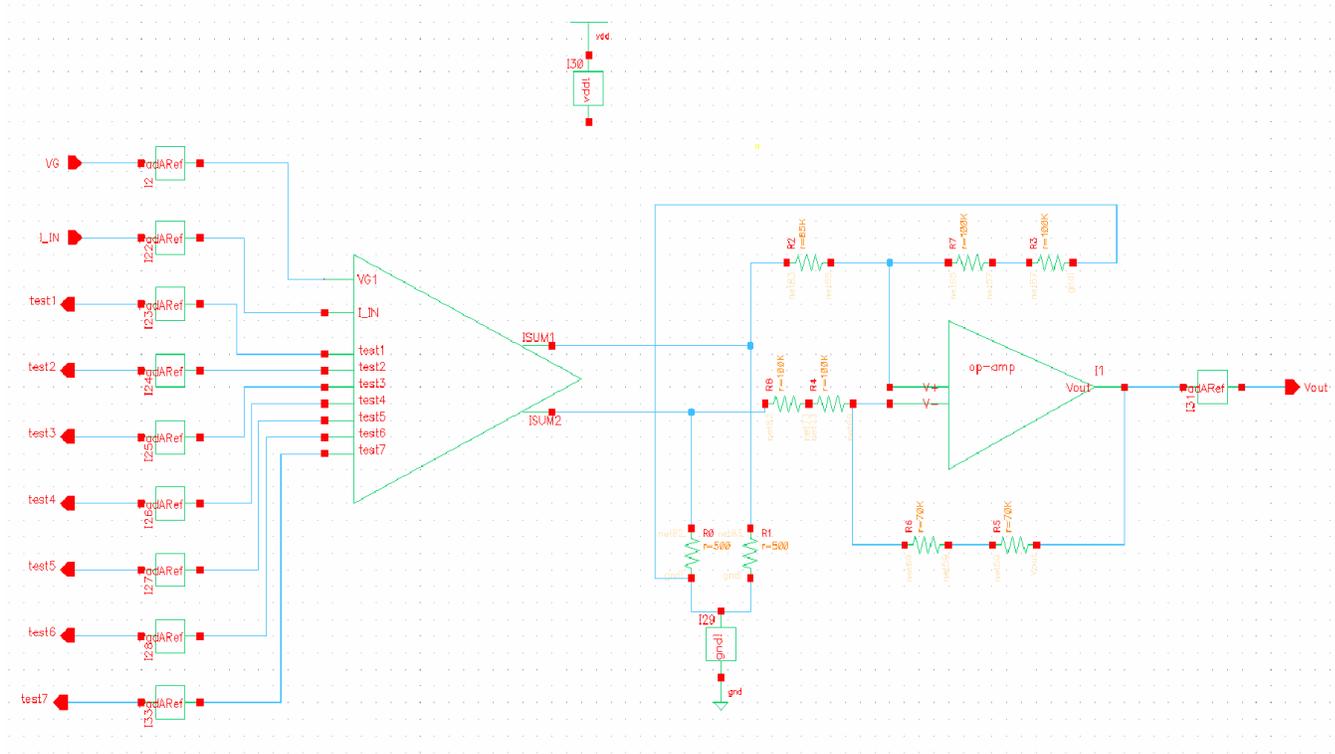


Figure 4.16: 120 dB Pseudo Logarithmic Amplifier Circuit

4.5.1 Final System Layout

The final layout is put together by connecting the layout of the cascaded amplifiers in figure 4.3 and the layout of the difference amplifier in figure 4.12 in a standard bond-pad structure shown in figure 4.17. There are five signal pins and seven test pins that is connected from the bond-pad to the outside pins through metal 2 layer. Both vdd and gnd are connected through metal 1 layer. The top-level chip layout shown in Figure above has been verified by the design rule check (DRC) and layout versus schematic (LVS) tools both before and after the stream out process. Input and output pins were selected according to package specifications for lowest parasitics available, and the pins for the rail voltages were selected for the highest parasitic capacitance. The final pin-out is displayed in Table 4.1 below; underlined rows are directly involved with the 120dB pseudo-logarithmic amplifier, all others correspond to test structures or no connect blocks:

Note: I_{out6} , I_{out1} , I_{out2} etc from the table 4.1 below = Current output from the 6th, 1st, 2nd current limiting amplifier from the cascaded configuration.

Pin Number	Pin Name	Functionality
1	test6	I_{out6}
2	N/A	N/A
3	test6	I_{out5}
4	N/A	N/A
5	N/A	N/A
6	N/A	N/A
7	N/A	N/A
8	N/A	N/A
9	N/A	N/A
10	N/A	N/A
11	N/A	N/A
12	N/A	N/A
13	N/A	N/A
14	N/A	N/A
15	N/A	N/A
16	N/A	N/A
<u>17</u>	VG	Bias Voltage
<u>18</u>	test4	I_{out4}
19	N/A	N/A
<u>20</u>	gnd!	Sytem ground
<u>21</u>	test3	I_{out3}
22	N/A	N/A
<u>23</u>	test2	I_{out2}
24	N/A	N/A
25	N/A	N/A
26	N/A	N/A
<u>27</u>	I _{in}	Input Current
28	N/A	N/A
29	N/A	N/A
<u>30</u>	test1	I_{out1}
31	N/A	N/A
<u>32</u>	V _{out}	Output Voltage
33	N/A	N/A
34	N/A	N/A
35	N/A	N/A
36	N/A	N/A
37	N/A	N/A
<u>38</u>	test7	I_{out7}
39	N/A	N/A
<u>40</u>	gnd!	Chip ground connection

Table 4.1: Project Specifications.

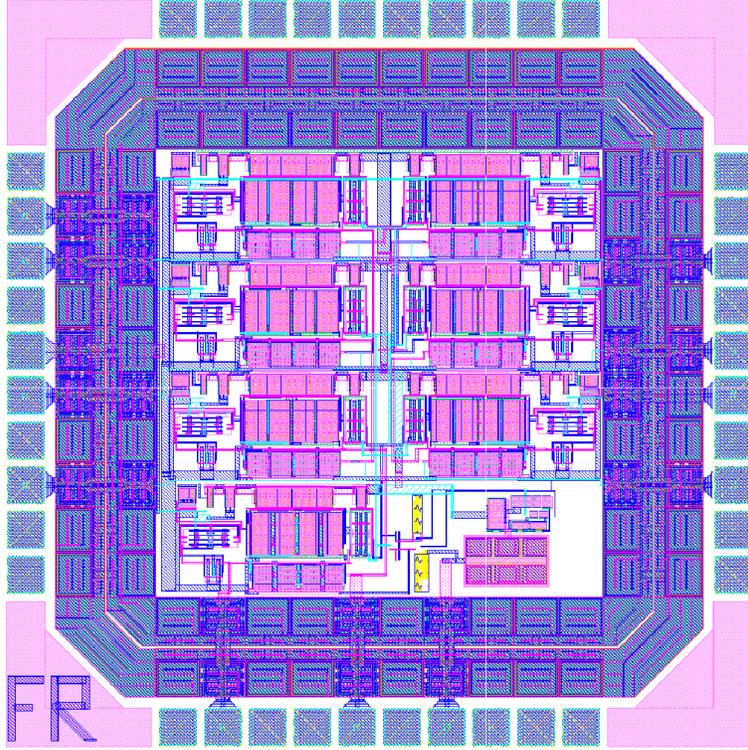


Figure 4.17: 120 dB Pseudo Logarithmic Amplifier Layout

4.5.2 Final System Test Circuit

The system test circuit is shown in figure 4.18. A voltage source is used for the bias, a current source is used for the I_{in} , along with the power supply that provides 5 VDC. The 20pF capacitor is used for as a load to get the output voltage. The symbol "120 dB Log Amp" created in cadence is the pseudo logarithmic amplifier and the unit under test.

4.5.3 120dB Pseudo Logarithmic Test Plot

The output of the log amplifier is a single ended voltage specified in section 1.2. The system output is shown in figure 4.19. The plot here shown from 1.25 volts to 4.25 which is close to the required specification.

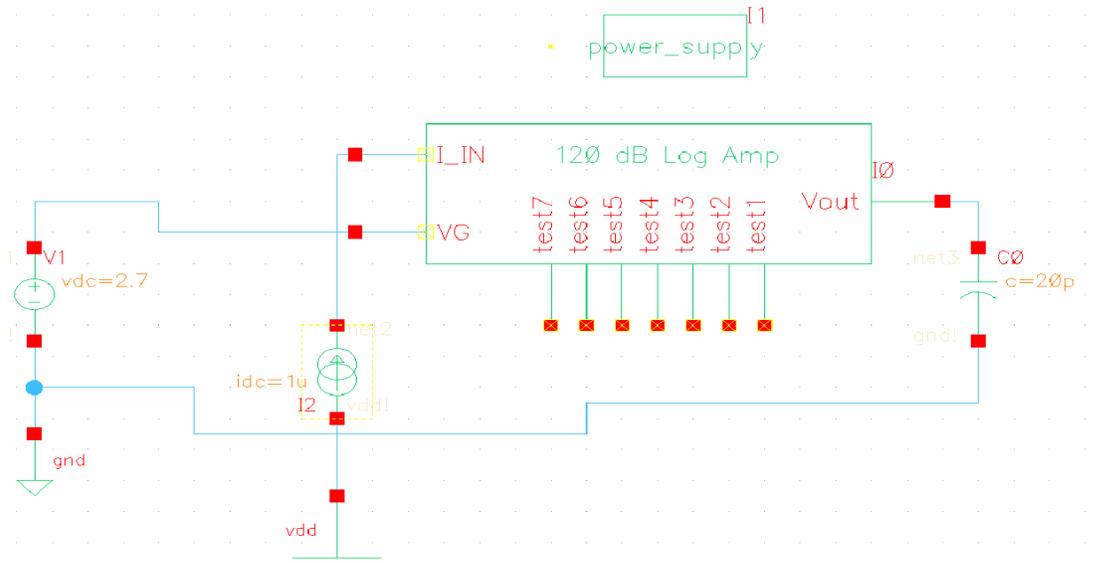


Figure 4.18: Test Circuit Pseudo-Logarithmic Amplifier

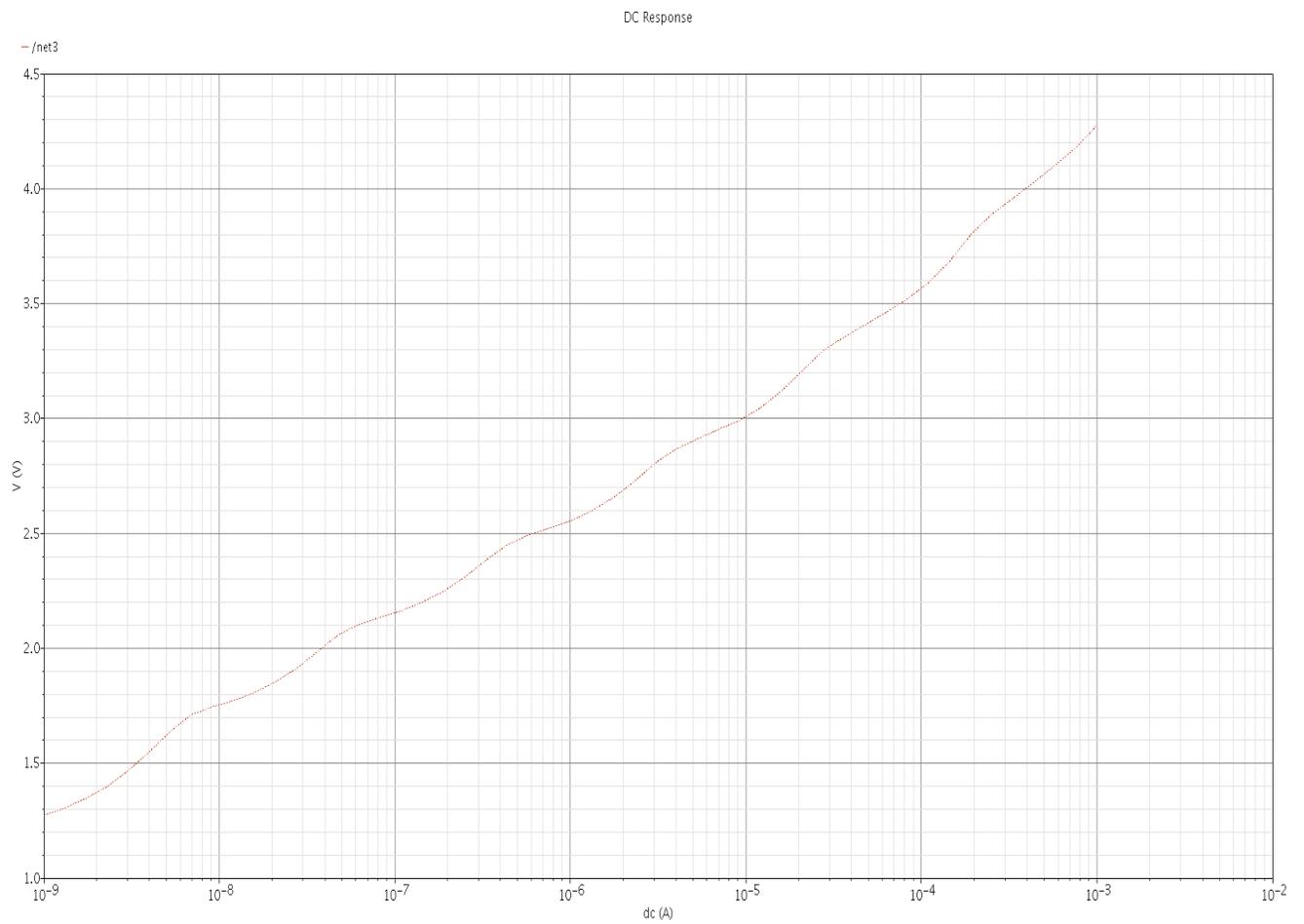


Figure 4.19: 120 dB Pseudo Logarithmic Amplifier Output Plot

Chapter 5

On Chip Test

A test block diagram is provided in the figure 5.1 below. R1 is a variable resistor to create the range of I_{in} from 1nA to 1mA. Resistors R2 and R3 values will be calculated. Resistors R4 to R10 can each be 1K. The zener diode is there to make sure the bias voltage gets clamped at $\cong 2.7$ volts. The capacitor C1 is 20pF. The supply voltage is 5VDC. The following tables that was mentioned in subsection 2.2.3 will be used to check the validity of the pseudo logarithmic amplifier chip. We will have the following signal as well as the voltage plot to validate the log functionality of the chip. They are

- I_{out}
- V_{out}

Through the data provided in these plots, we will check for a given current input I_{in} if we are getting the corresponding current outputs I_{out} in each stages of the cascade. To check for the V_{out} we will refer to the plot in figure 4.19.

5.1 Recommendation for Future Work

The following aspects or criteria will be added to a eleven stage chip that is due for my final thesis project.

- Temperature Effect
- Band Gap Reference
- Self Biasing Circuit
- Compensation Circuit for stability

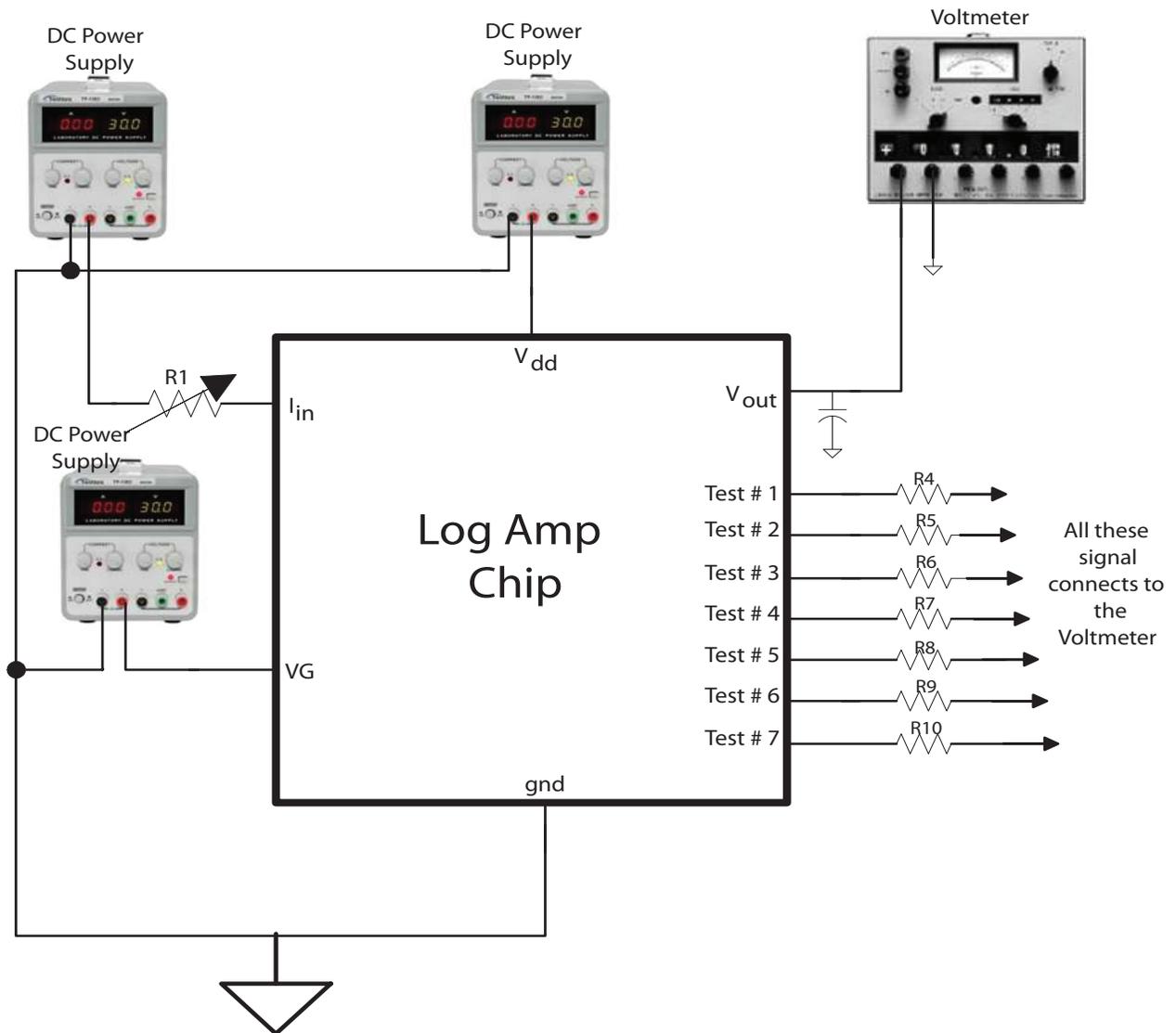


Figure 5.1: Block Diagram for Testing Log Chip

Stage	I _{in} (nA)	I _{out} (nA)	I _{sum_2} (mA)	I _{sum_1} (mA)	I _{LOG} (mA)
1	1	9	0.4999995	0.5000005	0.000001
2	9	90	0.499995	0.500005	0.0000095
3	90	900	0.49995	0.50005	0.000095
4	900	9000	0.49955	0.50045	0.00095
5	9000	90000	0.4955	0.5045	0.009
6	90000	900000	0.455	0.545	0.09
7	900000	9000000	0.05	0.95	0.9
-	-	-	-	Σ	1.000055 \approx 1

Table 5.1: Current Calculations for Seven Stage Cascade, I_{in}=1nA

Stage	I _{in} (nA)	I _{out} (nA)	I _{sum_2} (mA)	I _{sum_1} (mA)	I _{LOG} (mA)
1	10	90	0.499995	0.500005	0.00001
2	90	900	0.49995	0.50005	0.00009
3	900	9000	0.49955	0.50045	0.0009
4	9000	90000	0.4955	0.5045	0.009
5	90000	900000	0.455	0.545	0.09
6	900000	9000000	0.05	0.95	0.9
7	9000000	90000000	0.05	0.95	0.9
-	-	-	-	Σ	1.9 \approx 2

Table 5.2: Current Calculations for Seven Stage Cascade, I_{in}=10nA

Stage	I _{in} (mA)	I _{out} (mA)	I _{sum_2} (mA)	I _{sum_1} (mA)	I _{LOG} (mA)
1	1	9	0	1	1
2	9	10	0	1	1
3	10	10	0	1	1
4	10	10	0	1	1
5	10	10	0	1	1
6	10	10	0	1	1
7	10	10	0	1	1
-	-	-	-	Σ	7

Table 5.3: Current Calculations for Seven Stage Cascade, I_{in}=1mA

Bibliography

- [1] Z. Richards, “DESIGN OF A 120dB PSEUDO-LOGARITHMIC AMPLIFIER IMPLEMENTED IN THE AMI 0.5m PROCESS,” May 2007.
- [2] K. Koli, K.; Halonen, “A 2.5 v temperature compensated cmos logarithmic amplifier,” *Custom Integrated Circuits Conference 1997 Proceedings of the IEEE*, pp. 79–82, May 1997.
- [3] L. M. Gray, Hurst, *Analysis and Design of Analog Integrated Circuits*. USA: Wiley, 5th ed.
- [4] K. H. Yuhua Cheng, Mansun Chan, “Bsim3v3 manual,” 1996.

Appendix A

Mathlab Scripts

Appendix A1 contains the MATLAB code used to model the relationship between power consumption and the different configurations of gain and number of stages that yield the same dynamic input range.

```
1 Faisal Rahman
2 ECE 547, Decenmer 2011
3 Calculating the Gain/Number of Stages for the Current Limiting Amplifier
4 N=4:0.1:50; % choocing the range from 4 otherwise for N<4 the gain, G=4 goes
5 %high and power goes very high
6 P=0.0033 .* (-1+ (3.5.*N) + N.* (10.^(6./(N-1))));
7 y = diff(P);
8 figure
9 hold on
10 grid on
11 xlabel('Number of stages')
12 ylabel('Power')
13 title('Power vs Number of Stages')
14 plot(N,P, 'Linewidth',2)% showing power and the corrsponding stages
15 %
16 M=4.05:.1:50; % Since N has 460 + 1 =461 stages. M is 1 less than N
17 figure
18 grid on
19 xlabel('Number of Stages')
20 ylabel('Power')
21 title('1st Dervative of the Power vs to Number of Stages')
22 hold on
23 plot(M,y, 'Linewidth',2) % 1st derivative; so this line which is the slope of the
24 %should intersect plot (N,P)at the lowest power with the
25 %corrsponding number of stages, here it it 10
```