Low Noise Operational Amplifiers

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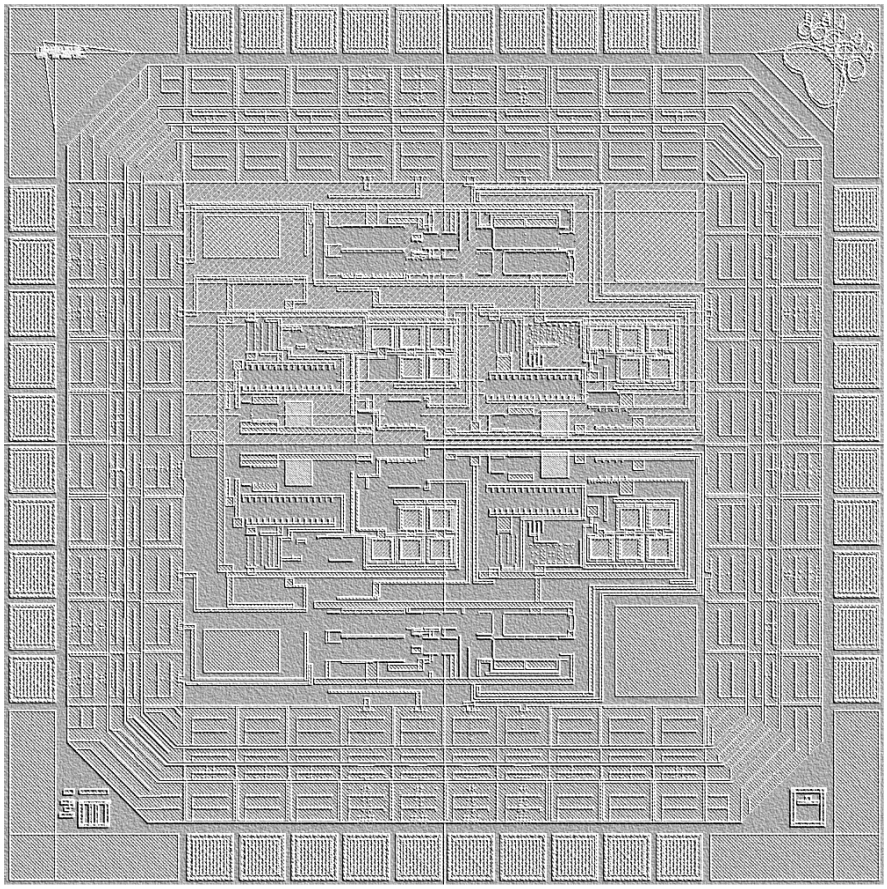

ECE 547- Project Report
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Abstract

This project report presents the design, layout, simulation and comparison results of two different low noise Operational Amplifier (Op-Amp) structures. Emphasis has been placed on the comparison of the Op-Amp performance. The two Op-Amps including a new structure and a Folded-Cascode structure were designed and laid out in 0.5 micron technology. While the literature emphasizes the reduction of flicker noise, the two structures in the project minimized the flicker noise and thermal noise simultaneously. Our results show that the two Op-Amps have comparable performance in simulation. Experimental testing needs to be carried out for further evaluations.

Acknowledgements

The author would like to thank Dr. David Kotecki for his insightful guidance and patience throughout this project. The author appreciates Gregory Flewelling, Jason Beaulieu, Zachary Richards and Taoufiq Bellamine for their interesting discussions.

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Part I

1. Background

Low noise Op-Amp has applications in proposed gene sequencers. Figure 1.1 shows the schematic of a gene sequencer. When a single strand DNA passing through the nano pore, the sequencer generates a modulated signal in the range of several pico-amps to a nano-amp, and the bandwidth can be up to 10MHz. In order to detect such a weak signal, an ultra low noise Op-Amp is needed.

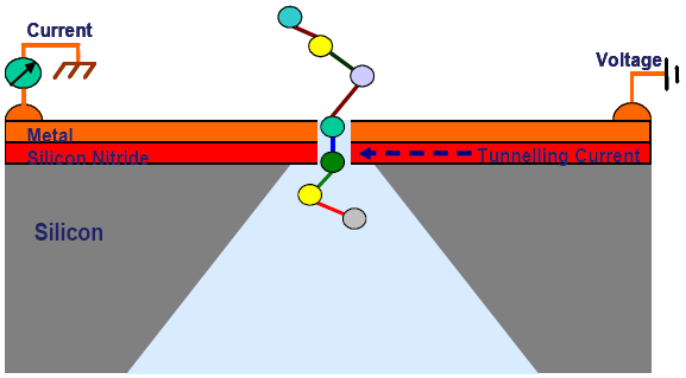

Figure 1.1: Schematic of a gene sequencer [1]

In MOSFET devices, there are two noise sources, which are flicker noise (below 1MHz) and thermal noise. Figure 1.2 shows the PSD of both types of noise on the same axis such that the flicker noise and the thermal noise can be distinguished. The corner frequency is where both PSDs of the flicker and thermal noise are equal to each other. In Figure 1.2, it is illustrated that the flicker noise is inversely proportional to the frequency and is dominant at low frequency. The thermal noise is independent of the frequency so that when flicker noise is insignificant at high frequency it dominates. In the sub-micron CMOS process, the flicker noise might be significant at frequency well into the megahertz range. For the nano pore gene sequencer

application, the bandwidth is estimated to be between 1MHz and 10MHz. In such a frequency range, the thermal noise is dominant. However, the flicker noise tail will overlap the thermal noise and increase the noise floor. Both types of noise need to be considered in this bandwidth if the Op-Amp is implemented by the sub micron CMOS process.

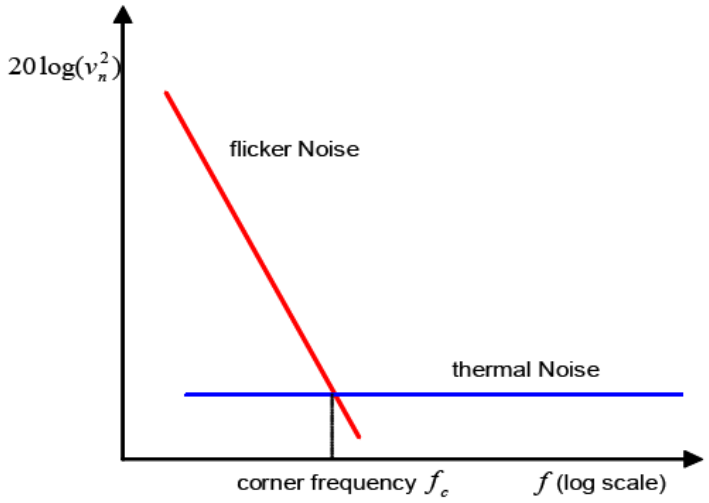

Figure 1.2: PSD of both types of noise [1]

2. Objective

The objectives for the project are (1) to design the new structure and Folded-Cascode Op-Amps in 0.5 micron process with the consideration of reducing both flicker noise and thermal noise, (2) to make it capable of operating in the frequency range of 1-10MHz, (3) to maximize the unity gain bandwidth and DC gain, (4) to compare the performance of the two structures.

3. Overview

These Op-Amps are designed based on 0.5 micron CMOS process with 5 volts supply voltage. The Cadence environment was used for the design, layout, and simulation. The final chip will be implemented through MOSIS, with AMI's C5N process. The device will be packaged in a 40-pin ceramic DIP and tested in the Fall of 2007.

Part II

4. Circuit Components—Schematics

Figure 4.1 shows the test schematic of Op-Amps. The bias circuit provides the bias current and voltage to the Op-Amps. The inputs of the two Op-Amps are connected to each other so that they share the same input signal. Their output signals are then collected separately and compared. This setup is designed specifically for the purpose of performance comparison.

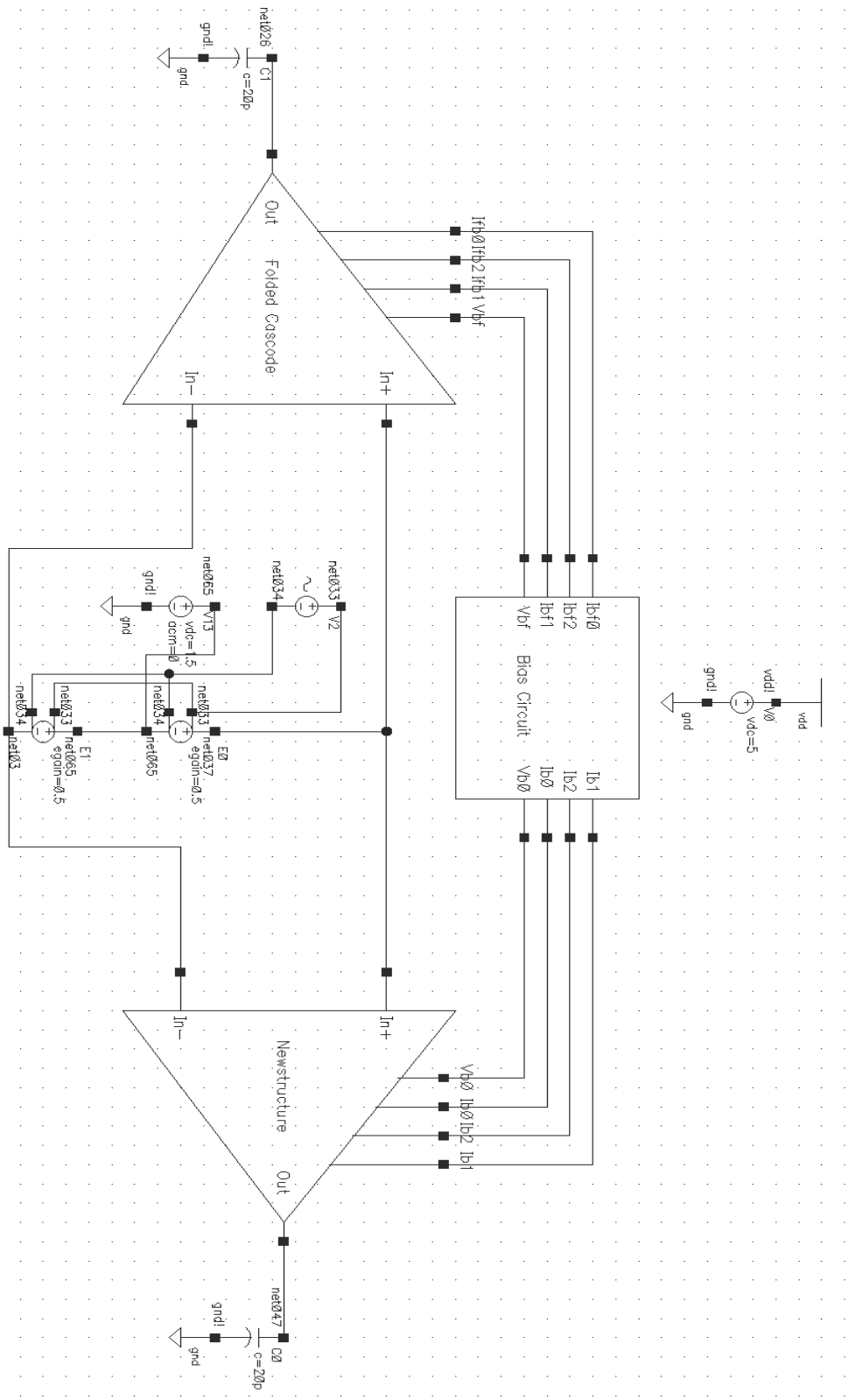

Figure 4.1: Test schematic of the Op-Amps

The test schematic illustrates that the circuit consists of three major components. They are the new structure Op-Amp, the Folded-Cascode Op-Amp, and the bias circuit. In the following sections, these three components will be described and discussed in details. The complete view of schematic can be found in Appendix A.

4.1 New structure Op-Amp design

Figure 4.2 shows the first stage of the new structure Op-Amp. This structure combines the advantage of a fully differential pair with an active current source load and a differential pair with a current mirror load. The active current source M3 and M4 source the possible maximum current for the input pair to reduce the thermal noise. The current M7 and M8 combine with the transconductance of the input pair to define the DC gain. Stage of M5 and M6, which is the cascode stage, reduces the Miller effect, thereby increase the bandwidth of the amplifier. This stage increases the output resistance looking into the drain of M6 and therefore increases the gain of the differential pair. It also reduces the short channel variation of the input stage. The bias current of input pair is ratioed between $M_{3,4}$ and $M_{7,8}$. $M_{3,4}$ sources most of the bias current. This structure has advantage of increasing the small-signal gain without deteriorating the noise performance. A large bias current, e.g. 3mA, for the high aspect ration input pair was chosen for improving the bandwidth, lowering the flicker noise, and achieving higher DC gain.

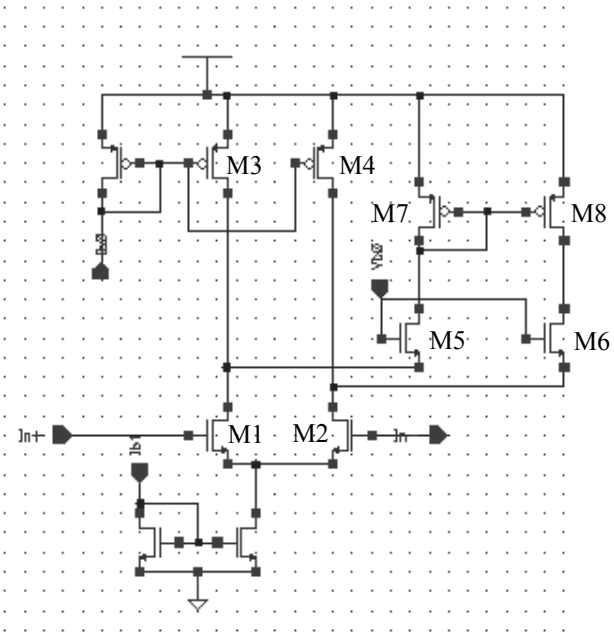

Figure 4.2: First stage of the new structure Op-Amp

Figure 4.3 shows the noise model for the new structure. The noise contribution of each gate is referred back to their own gate input. Symmetry has been assumed in this model, i.e. the noise contribution of M1, M3, M5 and M7 are the same as those of M2, M4, M6 and M8.

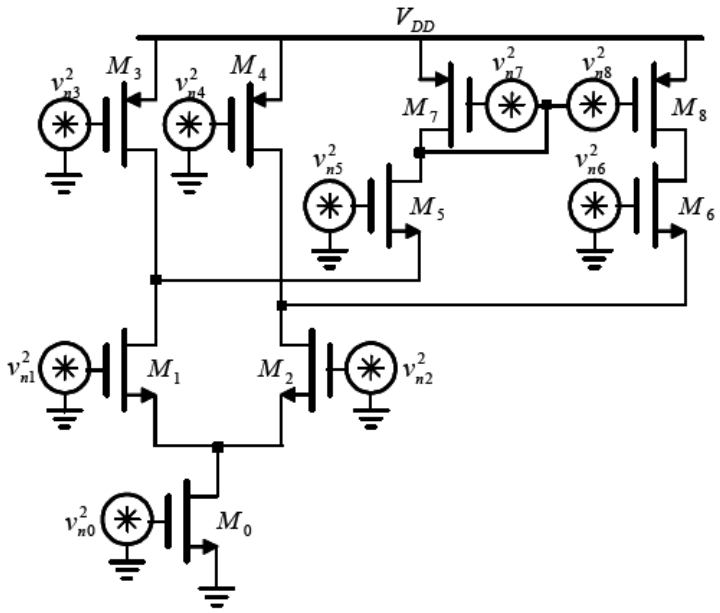

Figure 4.3: Noise model for the new structure [1]

Figure 4.4 shows the small signal noise model for the input stage of $M_{1,2}$. We have omitted the parasitic effect and the output noise from M2 is:

$$v_{no2} = g_{m2} r_8 v_{n2} \approx -g_{m2} r_0 v_{n2} \tag{4.1}$$

Where r_0 is the small signal output resistance of the circuit in Figure 4.2. Noise contribution of the active current source load stage $M_{3,4}$ is similar to $M_{1,2}$. We can get:

$$v_{no4} = g_{m4} r_8 v_{n4} \approx -g_{m4} r_0 v_{n4} \tag{4.2}$$

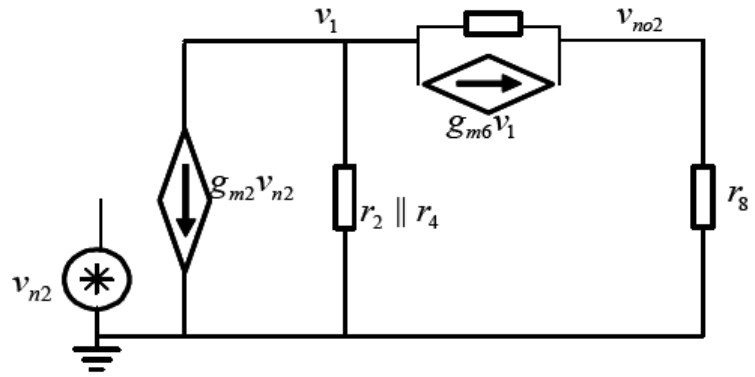

Figure 4.4: Small signal noise model for the input stage of $M_{1,2}$ [1]

The small signal model for $M_{7,8}$ is shown in Figure 4.5. The noise contribution from M8 is approximately by:

$$v_{no8} = g_{m8} r_8 v_{n8} \approx -g_{m8} r_0 v_{n8} \tag{4.3}$$

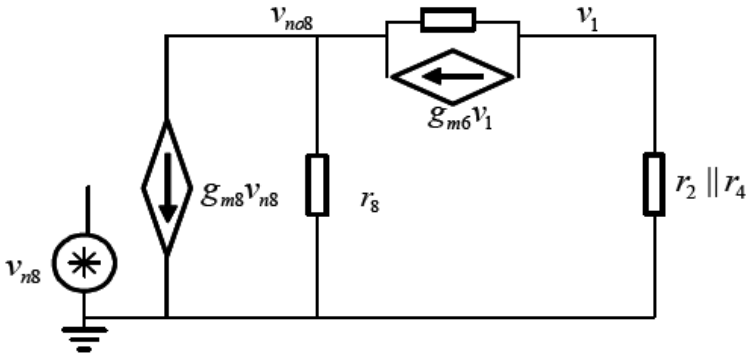

Figure 4.5: Small signal model for $M_{7,8}$ [1]

The small signal noise model for the cascode stage $M_{5,6}$ is shown in Figure 4.6. And the noise contribution from M6 is approximately by:

$$v_{no6} = \frac{-g_{m6} r_6 r_8}{r_6 + r_8 + g_{m6} r_6 r_2} v_{n6} \approx \frac{r_8}{r_2} v_{n6} \tag{4.4}$$

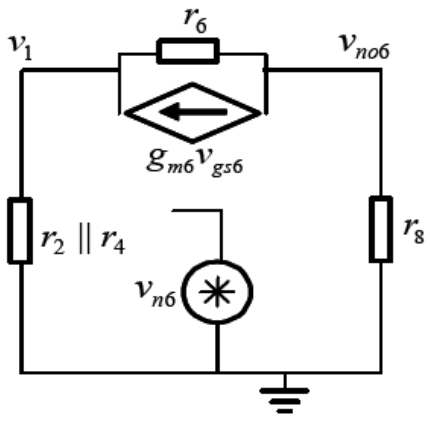

Figure 4.6: Small signal model for $M_{5,6}$ [1]

Since this noise is much smaller than those generated by current mirror loads, the input stage, and active current, it was omitted in the noise analysis. The noise contribution from the current bias M0 is also omitted due to the small value comparing to the other stage's input referred noise.

Combining the noise models and with some algebra, the flicker noise and thermal noise can be shown:

$$v_{flicker}^2(f) = \frac{KF_n}{\mu_n C_{OX}^2 W_2 L_2 f}[1 + \frac{KF_p}{KF_n}(\frac{L_2}{L_4})^2 \frac{I_{D4}}{I_{D2}} + \frac{KF_p}{KF_n}(\frac{L_2}{L_8})^2 \frac{I_{D8}}{I_{D2}}] \qquad (4.5)$$

$$v_{thermal}^2 = \frac{16kT}{3\sqrt{2\mu_n C_{ox}(W/L)_2 I_{D2}}}\left(1 + \sqrt{\frac{\mu_p (W/L)_4 I_{D4}}{\mu_n (W/L)_2 I_{D2}}} + \sqrt{\frac{\mu_p (W/L)_8 I_{D8}}{\mu_n (W/L)_2 I_{D2}}}\right) \qquad (4.6)$$

From the expressions above we can reduce the noise through optimizing the sizes and aspect ratios of the MOSFETs, selecting appropriate input MOSFET type for $M_{1,2}$, optimizing the bias current of the input pair.

We have chosen the NMOS as the input pair for three reasons. First, NMOS has larger mobility μ_n (2-3 times greater) than PMOS. According to Equation (4.6), NMOS has smaller thermal noise than PMOS. Second, the flicker noise could be dominant in

the submicron process at frequency greater than 1 MHz. NMOS has smaller flicker noise coefficient. Third, NMOS has higher transition frequency f_T than PMOS, which helps achieving a higher bandwidth.

We have chosen a large size $(W/L)_2$ for the input pair. Choosing channel length L of $M_{3,4}$ and $M_{7,8}$ larger than that of the input pair helps reducing the flicker noise. The aspect ratio of the input pair was chosen to be larger than those of $M_{3,4}$ and $M_{7,8}$ such that the thermal noise can be reduced. It should be noted that the input pair contributes most of the thermal noise and flicker noise by choosing such parameters for the FETs. The optimum gate length of $M_{1,2}$ is found to be 0.75μm in the 0.5 μm process by:

$$\frac{\partial v_{flic\,\mathrm{ker}}^2}{\partial L_2} = 0 \qquad (4.7)$$

Thanks to the new structure we can choose the bias current for the input up to 3 mili-amps for good noise performance without deteriorating the gain and voltage headroom at the output.

Overall, M1, M2, M3, M4 are responsible for the noise reduction and M1, M2, M5, M6, M7, and M8 are responsible for the DC gain. The DC gain and noise are often trade off in differential pair with current mirror load. However, for this new structure they can be optimized independently.

4.2 Folded-Cascode structure Op-Amp

Figure 4.7 shows the schematic diagram for the Folded-Cascode structure. This structure is similar to the new structure Op-Amp. The differences are: M5 and M6 have been changed from NMOS to PMOS; current mirror load M7 and M8 have been connected to the ground instead of Vdd. Due the similarity of these two structures, the noise models for both of them are identical. However, by examination, the new structure has better noise performance than the Folded-Cascode one, provided the

current goes through M3 and M4 is the same for both of the structures. In the Folded-Cascode structure, $I_{FM4}=I_{FM2}+I_{FM8}$, while in the new structure, $I_{M2}=I_{M4}+I_{M8}$. We have assumed that $I_{M4}= I_{FM4}$, so that $I_{M2}>I_{FM2}$. Because of the larger of the bias current going through the input, the smaller the thermal noise, the new structure has better noise performance in theory.

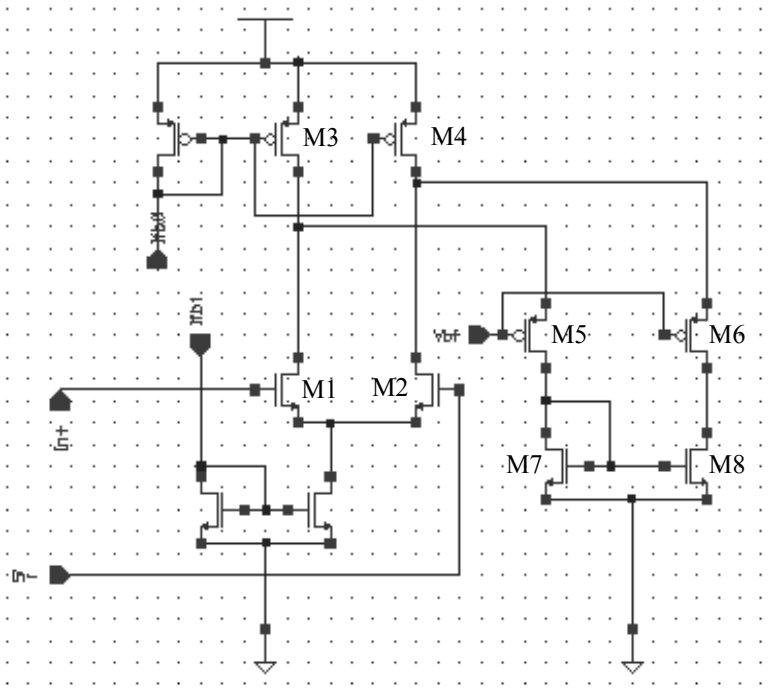

Figure 4.7: Schematic diagram for the Folded-Cascode structure

Due to one of the objectives that we want to compare the performance of the two Op-Amps, the types, sizes and aspect ratios of the Folded-Cascode have chosen to match with the new structure Op-Amp.

Figure 4.8 and Figure 4.9 show the Op-Amp with a second stage, a common source amplifier. A Miller compensation scheme is used in the two-stage Op-Amp to achieve good phase margin.

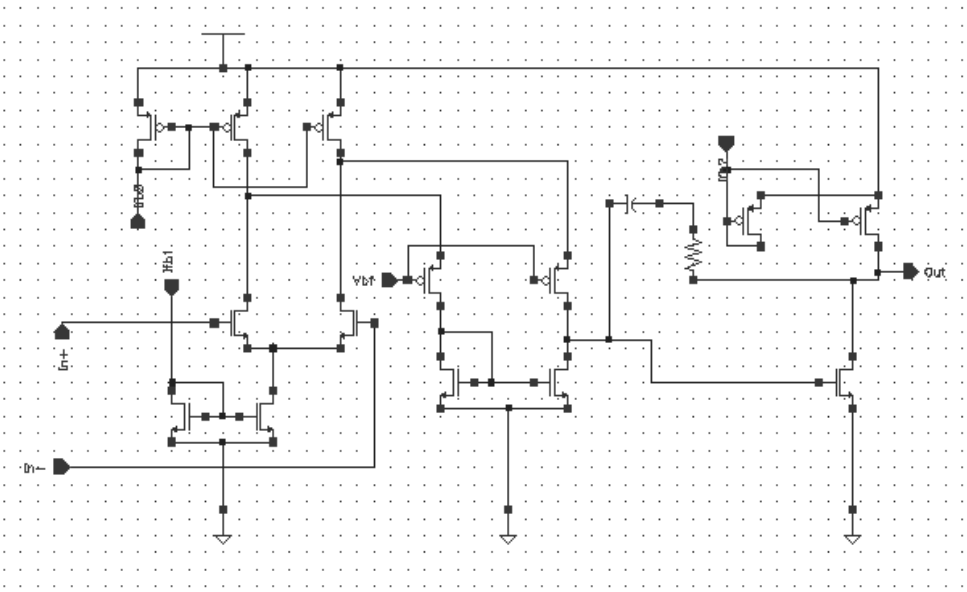

Figure 4.8: Two stage Folded-Cascode Op-Amp

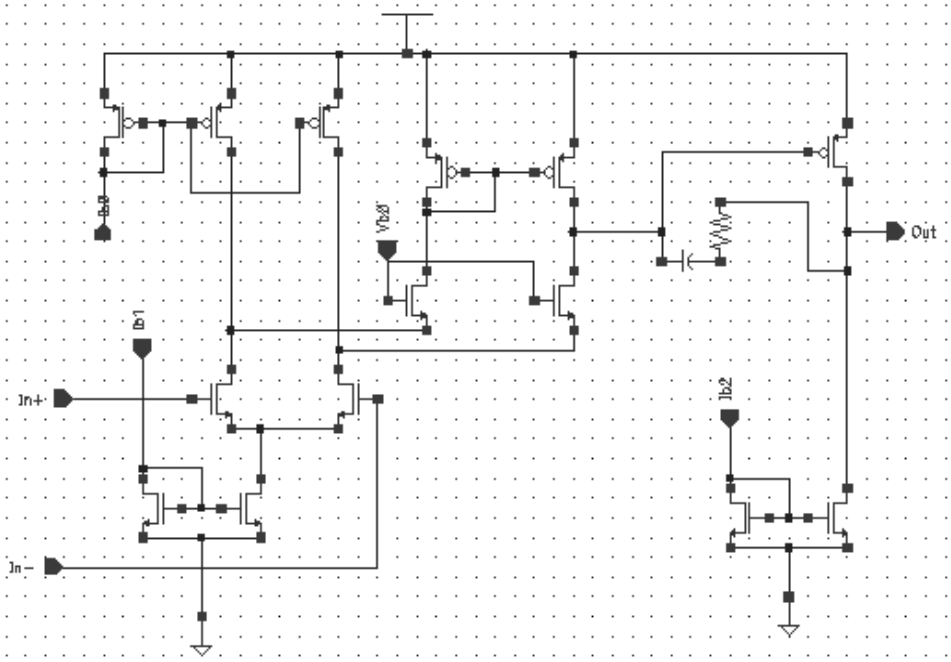

Figure 4.9: Two stage new structure Op-Amp

4.3 Bias Circuit

Figure 4.10 shows the bias core for the bias circuit. This bias circuit has good PSRR performance because the currents through $M_{b3,b4}$ are not sensitive to the supply voltage to the first order. M_{b5} is a long channel device and $M_{b5,b6,b7}$ consist of the start-up circuit.

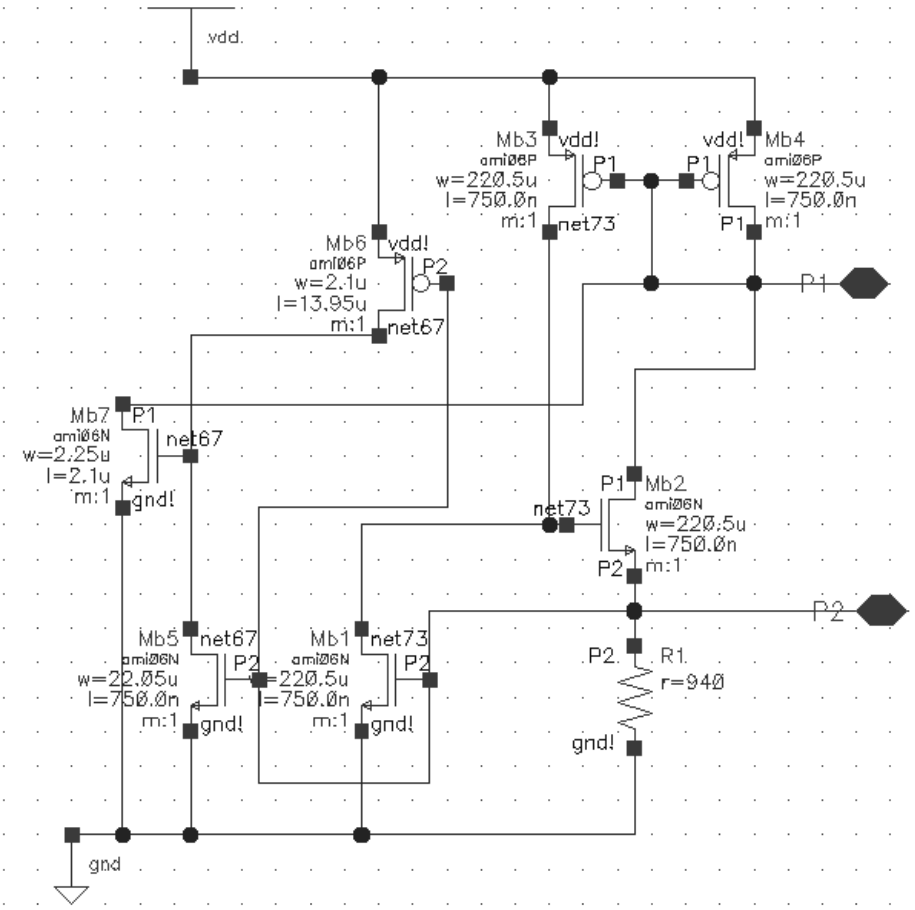

Figure 4.10: Bias core for the bias circuit

Figure 4.11 shows the entire bias circuit. Current mirror is used to input or output bias current, while resistor network is used to provide voltage bias.

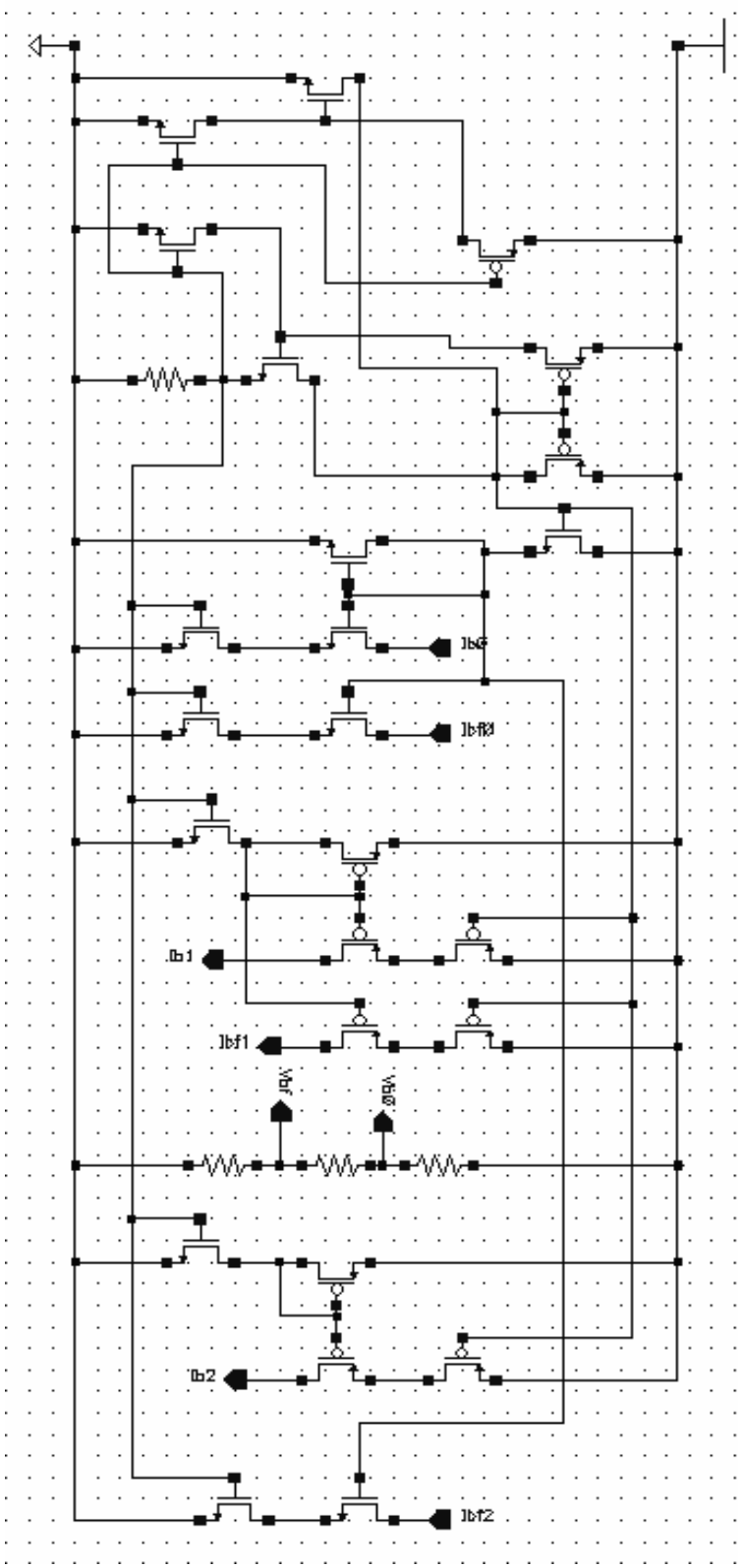

Figure 4.11: Entire bias circuit

4.4 simulation results

Due to the lack of the noise model in the available Cadence, the noise simulation was unable to perform. However, the noise performance can be determined experimentally. We will address this issue in Chapter 7. The simulation was performed by biasing the input pair at 1.5V, feeding a small AC signal, collecting the output. Figure 4.1 shows the testing schematic.

Figure 4.12 shows the unity gain bandwidth of the Op-Amps with zero load. The flat gain shown in the figure is around 110dB. The unity gain bandwidth is 123.7 MHz. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

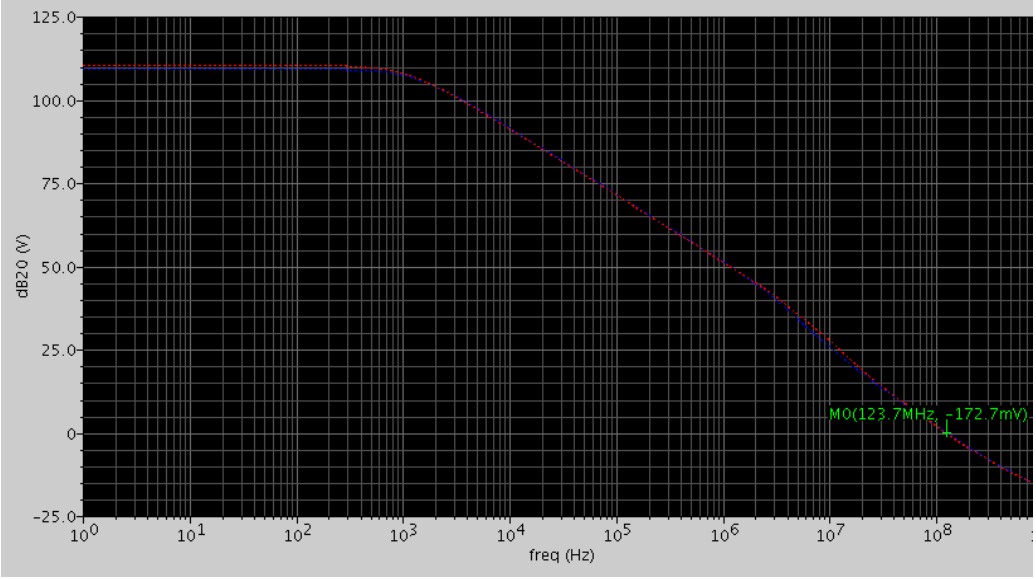

Figure 4.12: Unity gain bandwidth of the Op-Amps with zero load

Figure 4.13 shows the phase margin of the Op-Amps with zero load. The phase margin is about 65.9 Degrees. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

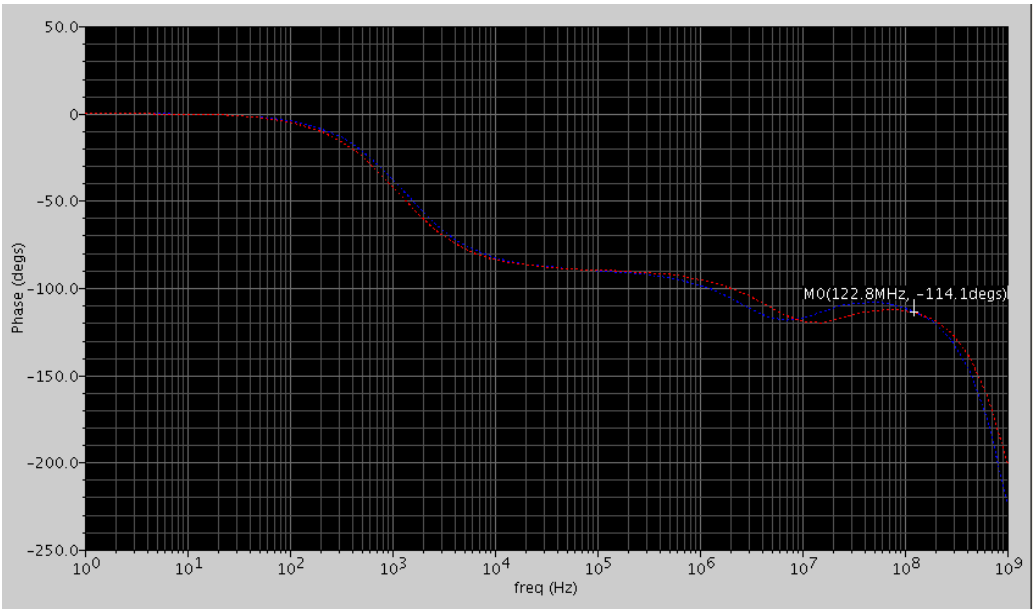

Figure 4.13: Phase margin of the Op-Amps with zero load

Figure 4.14 shows the unity gain bandwidth of the Op-Amps with 10pF load. The flat gain shown in the figure is around 110dB. The unity gain bandwidth is 100.9 MHz. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

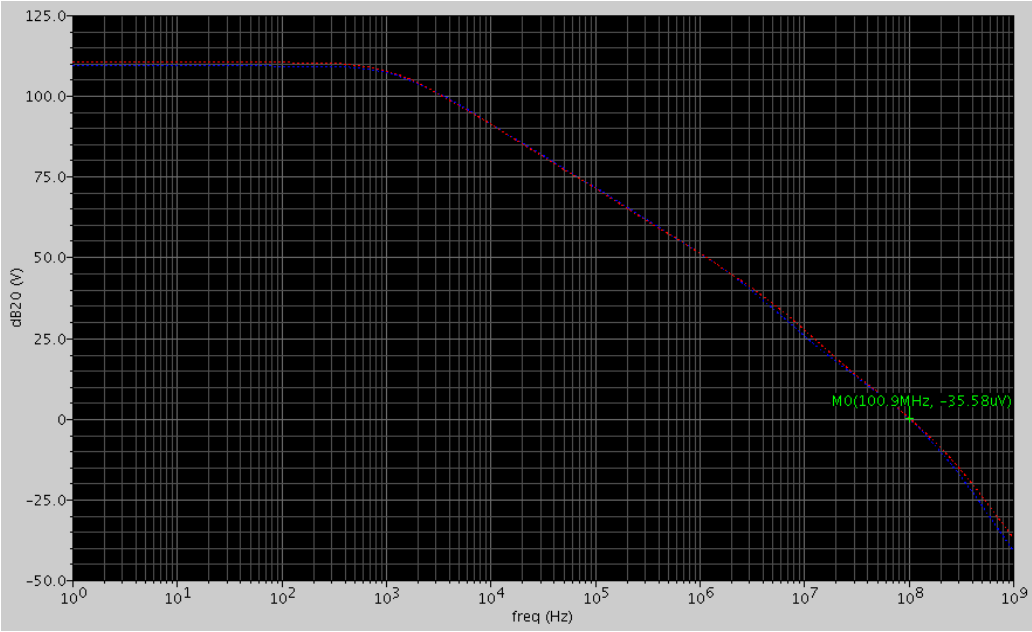

Figure 4.14: Unity gain bandwidth of the Op-Amps with 10pF load

Figure 4.15 shows the phase margin of the Op-Amps with 10pF load. The phase margin is about 33.1 Degrees. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

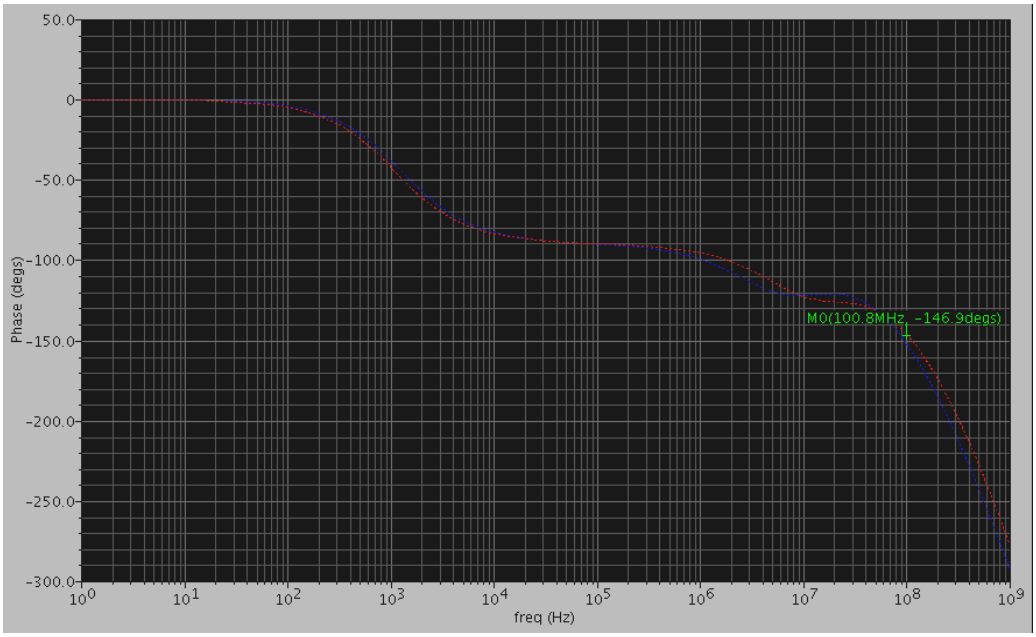

Figure 4.15: Phase margin of the Op-Amps with 10pF load

Figure 4.16 shows the unity gain bandwidth of the Op-Amps with 20pF load. The flat gain shown in the figure is around 110dB. The unity gain bandwidth is 86.36 MHz. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

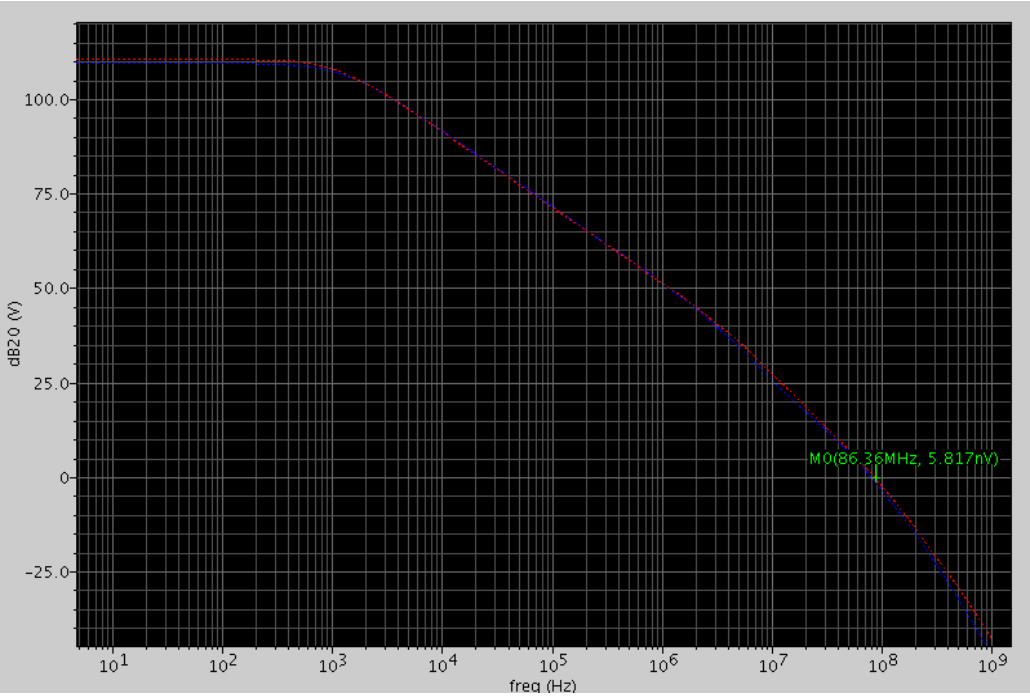

Figure 4.16: Unity gain bandwidth of the Op-Amps with 20pF load

Figure 4.17 shows the phase margin of the Op-Amps with 20pF load. The phase margin is about 18.6 Degrees. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

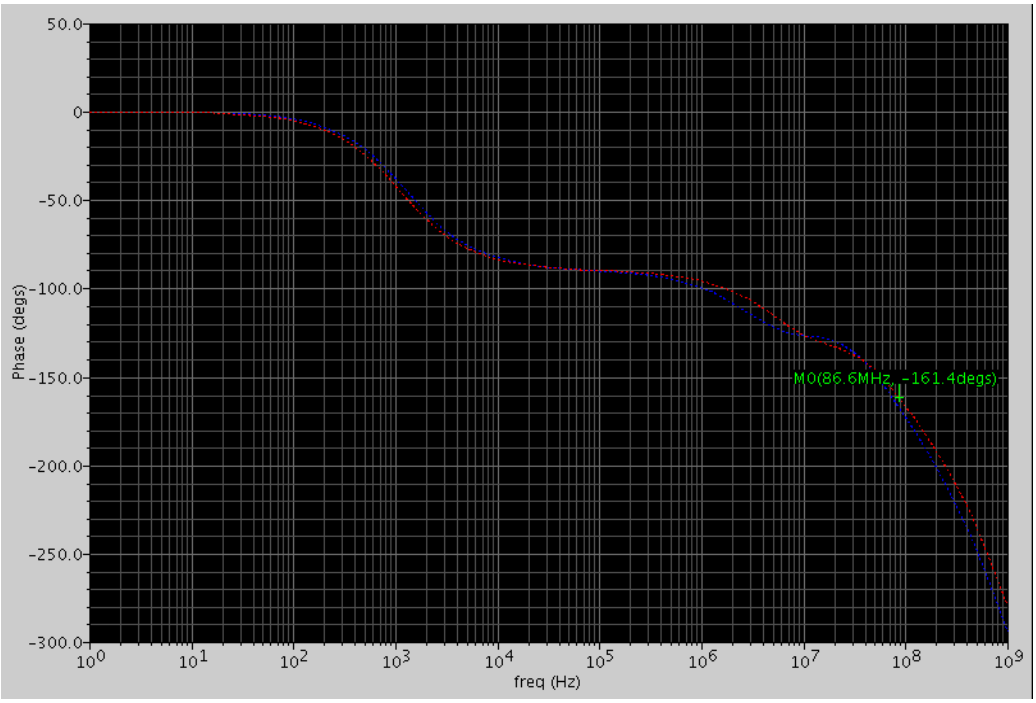

Figure 4.17: Phase margin of the Op-Amps with 20pF load

4.5 Pin-out table and probe-pad table

The die size available for the current design is 0.153” x 0.133” and it is packaged as a 40 pin DIP. Depending on the location some pins have higher parasitics than others. Table 1 shows the electrical characteristic of the 40 pin DIP. Pins were assigned based on the sensitivity of the signals. Vdd and Ground were assigned to pin20 and pin40 respectively. For low noise applications, Pins with the lowest parasitics i.e. pin10, pin11, pin30, and pin31, were used for the critical signals, such as output, and input signals, in order to minimize the noise that may be introduced by the pin trace. Table 2 shows the Pin-out table.

Table 1: Electrical characteristic of the 40 pin DIP

Pin	R (ohm)	L (nH)	C (pF)	t_{of} (ps)
1,20,21,40	0.217	8.18	5.32	209
2,19,22,39	0.177	7.92	4.39	187
3,18,23,38	0.154	7.34	3.37	157
4,17,24,37	0.110	6.48	2.34	1213
5,16,25,36	0.103	5.69	2.16	111
6,15,26,35	0.0661	4.37	1.43	79.0
7,14,27,34	0.0646	4.54	1.48	81.9
8,13,28,33	0.0498	3.69	1.05	62.3
9,12,29,32	0.0378	3.54	0.863	55.3
10,11,30,31	0.0247	3.15	0.660	45.6

Table 2: Pin-out and Pad-out

Pin#	Pad#	Purpose
3	3	“Vb0”, bias voltage input for the new structure (4.61V)
9	9	“Fout”, Op-Amp Output of the Folded-Cascode
10	10	“Fin+”, positive input of the Op-Amps
11	11	“Fin-“, negative input of the Op-Amps
12	12	“Nout”, Op-Amp Output of the new structure
16	16	“Fvbf”, 1.5 V output (can be used for biasing the input pair)
17	17	“Nvb0”, 4 V output
18	18	“Vbf”, Bias input for the Folded-Cascode (2.45V)
20	20	N/A (Pins not in the list are all unavailable)
21	21	Vdd (5V)
23	23	“Vbf1”, second device, Bias input for the Folded-Cascode (2.45V)
24	24	“Nvb0”, second device, 4 V output
25	25	“Fvbf1”, second device, 1.5 V output
29	29	“Nout1”, second device, Op-Amp Output of the new structure
30	30	“Fin-1”, second device, negative input of the Op-Amps
31	31	“Fin+1”, second device, positive input of the Op-Amps
32	32	“Fout1”, second device, Op-Amp Output of the Folded-Cascode
38	38	“Vb01”, second device, bias voltage input for the new structure
40	40	Ground

5. Layout

Figure B.1 shows the entire layout of the chip. The upper half consists of the bias circuit, the Folded-Cascode Op-Amp, and the new structure Op-Amp. Metal3 covers the upper half of the chip to provide shielding. The low half is the mirror of the upper half except that it does not have the Metal3 shielding. Comparison of the shielding effect can be achieved by such design.

In the following sections, the design considerations, post layout simulation and performance issues will be addressed. The complete view of layout can be found in appendix B.

5.1 Design considerations

The layout considerations for all components share some general characteristics such as reducing the cell size, minimizing the noise and introducing large number of contacts wherever possible. Multipliers and fingers were used wherever appropriate to help the cell in good shape and improve matching. Ground (GND) and Vdd rings were implemented to minimize the noise coupling between components. The design rule of at least 15% poly also require additional poly to be added if necessary.

In the following section, special considerations for this circuit will be addressed.

5.2 Layout techniques

Large devices can result in large parasitics if some layout issues are not considered. Figure 5.1 shows the layout of the input pair. This input pair has a large W/L, which would have large parasitics in both resistive and capacitive if fingers and multipliers are not used. More contacts along the width of both source and drain reduce the

diffusion resistance of the source and drain. The dummy poly strips on both sides of the device are used to help minimize the effects of undercutting the poly on the outer edges after patterning. If the dummy strips had not been used, the poly of the outermost gates would have been etched out more, resulting in a mismatch of the parallel devices.

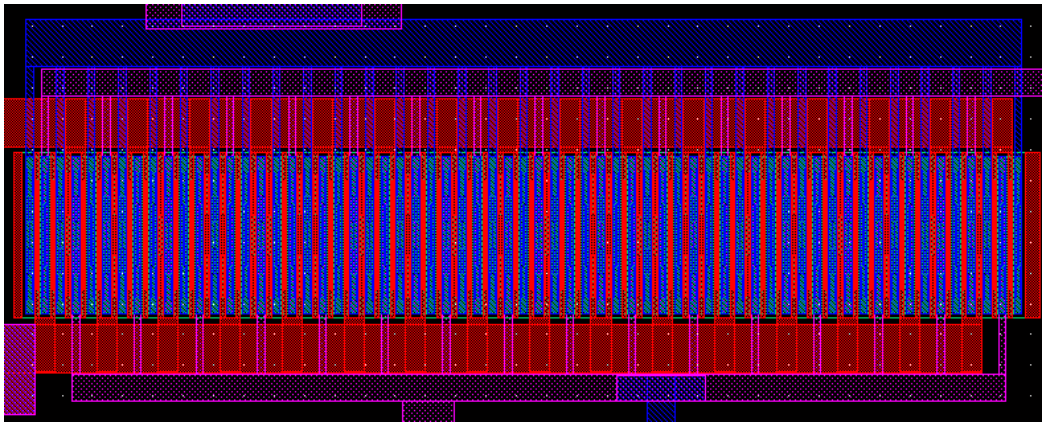

Figure 5.1: Layout of the input pair

Figure 5.2 shows the layout of the current mirror using interdigitation. When matching two devices, it is imperative that the devices are as symmetrical as possible. This requires that the devices need to be oriented in the same direction. Splitting the devices into parallel devices and interdigitizing them can distribute the process gradients across the devices, and thus improving matching.

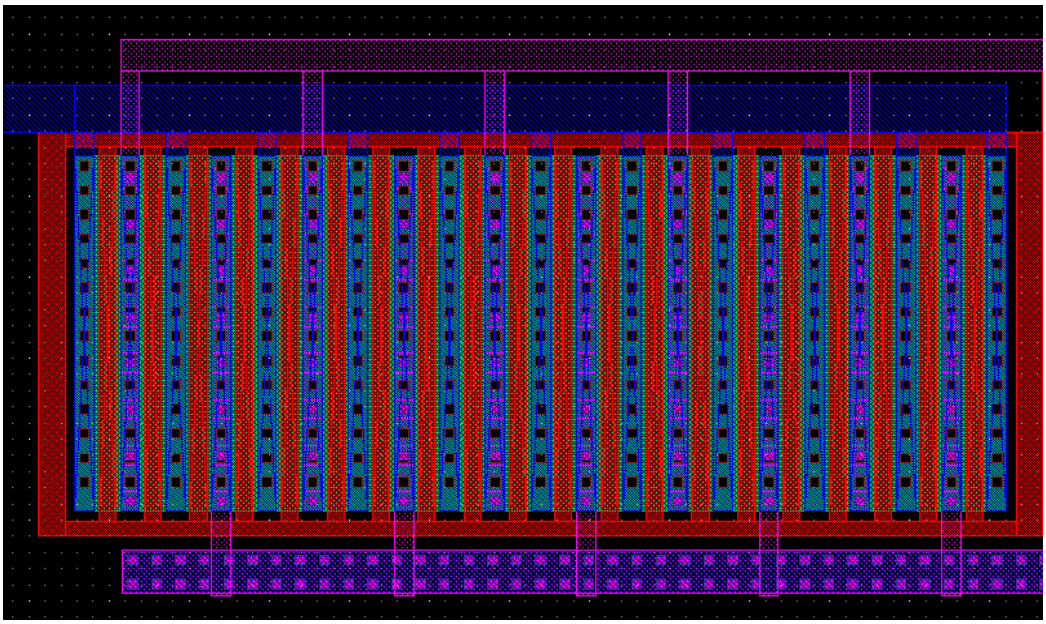

Figure 5.2: Layout of the current mirror using interdigitation

The gate of the modern CMOS device is made of polysilicon material often with a silicided surface layer instead of metal. The polysilicon silicided gate is more resistive than metal, and therefore noisier. In our low noise Op-Amp design, the wide transistors are used as input pair and the contribution of noise from the gate need to be minimized by proper layout. In Figure 5.2, each ends of the gate are connected together to reduce the overall gate resistance.

5.3 Post layout simulation

After layout, the circuit with parasitic was simulated. The following figures show some interesting results.

Figure 5.3 shows the unity gain bandwidth of the Op-Amps with zero load. The flat gain shown in the figure is around 105dB. The unity gain bandwidth is 212 MHz. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

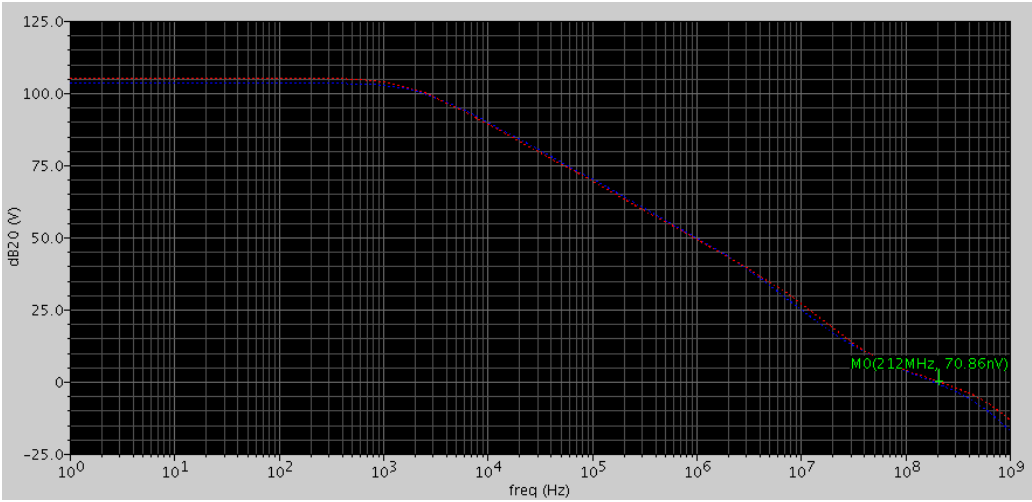

Figure 5.3: Unity gain bandwidth of the Op-Amps with zero load

Figure 5.4 shows the phase margin of the Op-Amps with zero load. The phase margin is about 91.51 Degrees. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

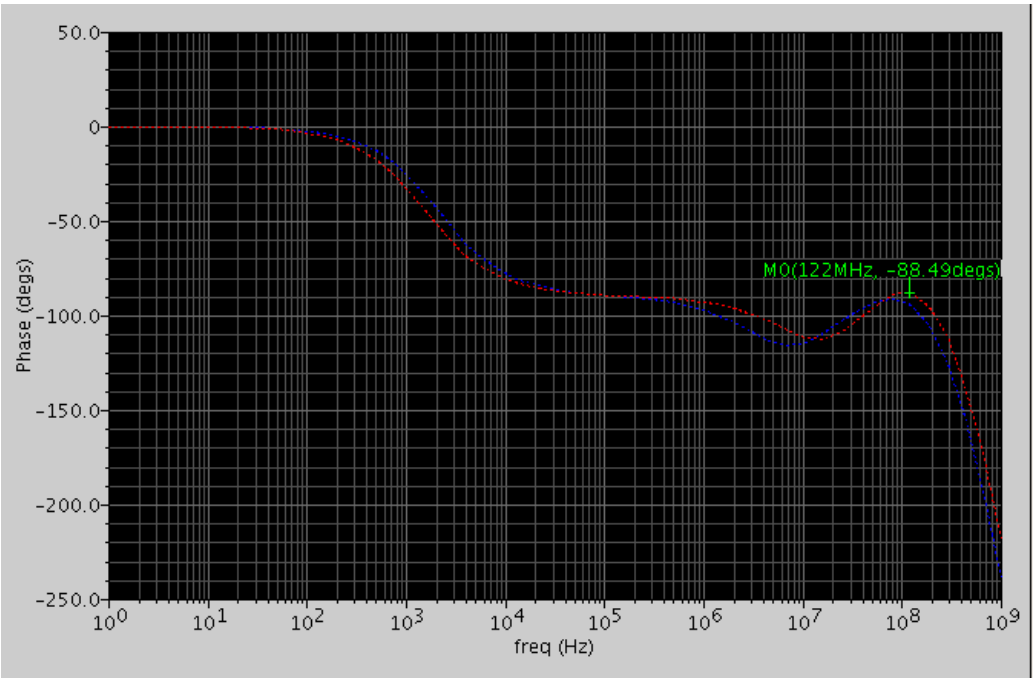

Figure 5.4: Phase margin of the Op-Amps with zero load

Figure 5.5 shows the unity gain bandwidth of the Op-Amps with 10pF load. The flat gain shown in the figure is around 105dB. The unity gain bandwidth is 133.3 MHz. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

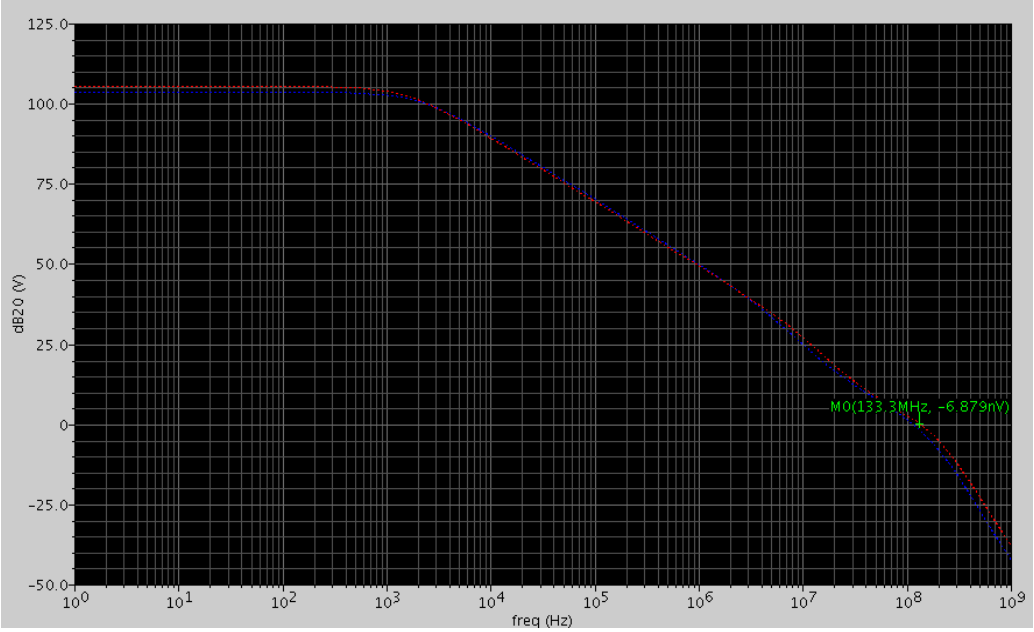

Figure 5.5: Unity gain bandwidth of the Op-Amps with 10pF load

Figure 5.6 shows the phase margin of the Op-Amps with 10pF load. The phase margin is about 35.2 Degrees. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

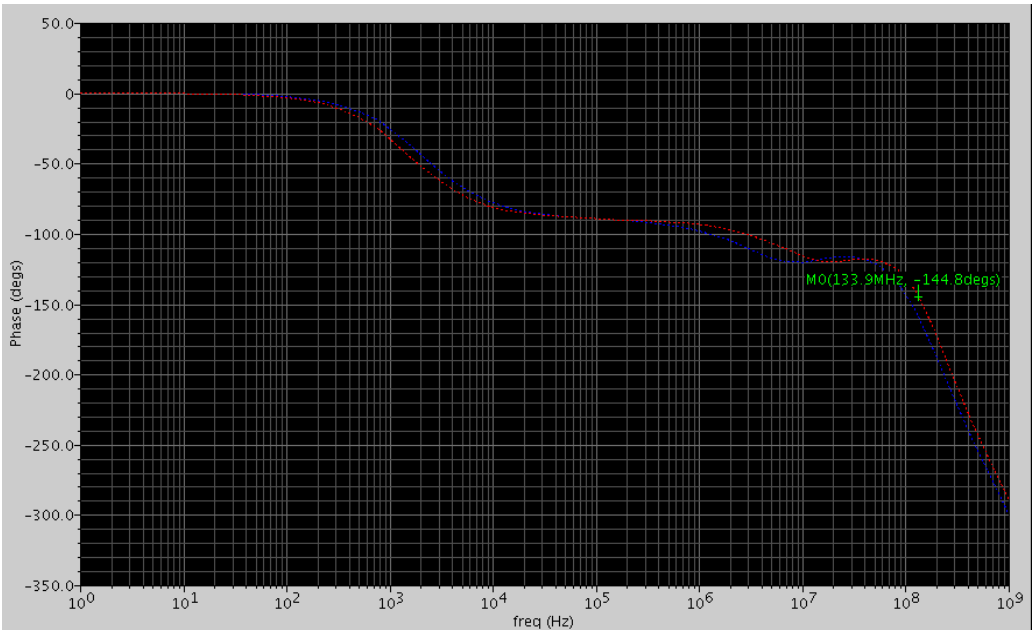

Figure 5.6: Phase margin of the Op-Amps with 10pF load

Figure 5.7 shows the unity gain bandwidth of the Op-Amps with 20pF load. The flat gain shown in the figure is around 105dB. The unity gain bandwidth is 93.67 MHz. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

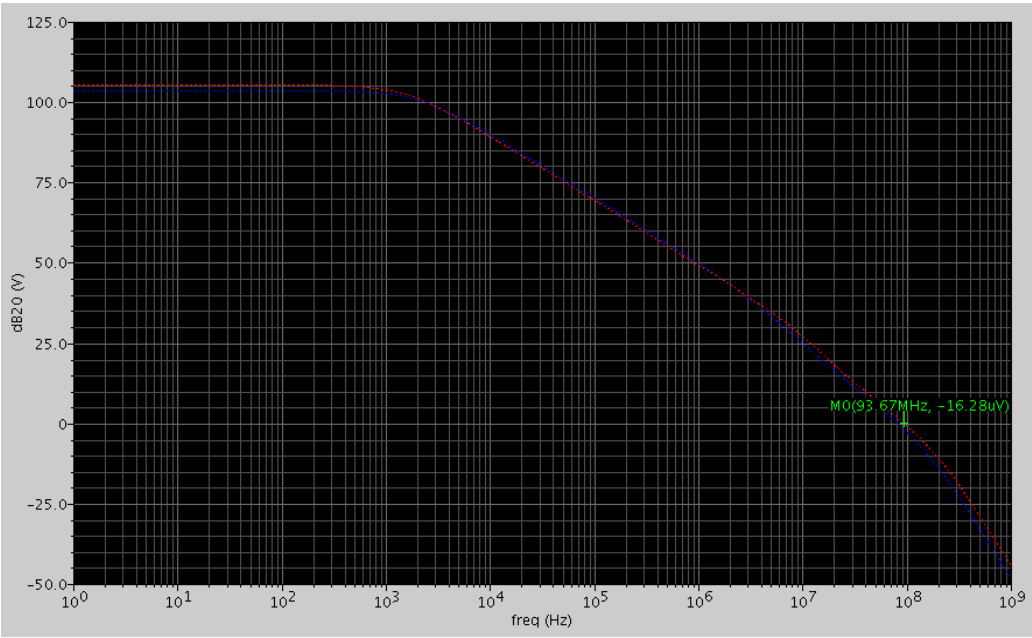

Figure 5.7: Unity gain bandwidth of the Op-Amps with 20pF load

Figure 5.8 shows the phase margin of the Op-Amps with 20pF load. The phase margin is about 28.3 Degrees. The red curve represents the Folded-Cascode structure, the blue one is for the new structure.

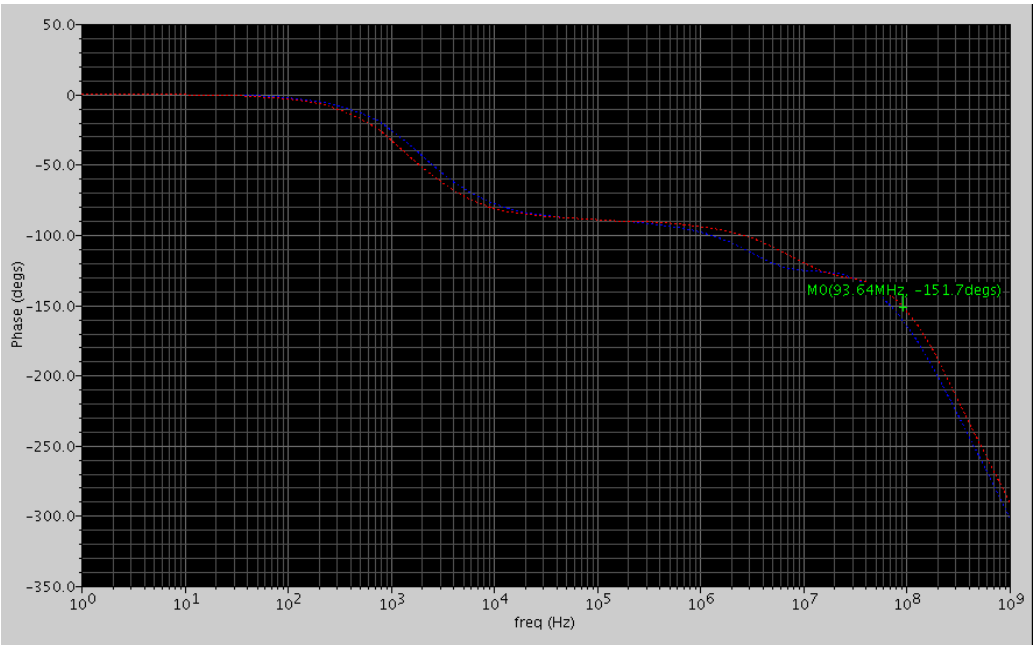

Figure 5.8: Phase margin of the Op-Amps with 20pF load

5.4 Performance issues

By comparing the simulation with and without the analog-extracted, we have found that the open loop gain of the Op-Amps has decreased ~5dB from ~110dB to ~105dB, the bandwidth and phase margin have increased. Table 3 shows the results with and without parasitics. Although the gain has decreased, the bandwidth and phase margin has improved with parasitics. It should be noted that the bias voltages for the Op-Amps have changed from internal bias, 1.5V for the Folded-Cascode structure and 4V for the new structure, to external bias, 2.45V for the Folded-Cascode structure and 4.64V for the new structure.

Table 3: Simulation results with and without parasitics

Output Load	Without parasitics		With parasitics	
	Bandwidth	Phase Margin	Bandwidth	Phase Margin
0 F	123MHz	65.9°	212MHz	91.51°
10 pF	100.9MHz	33.1°	133.3MHz	35.2°
20 pF	86.36MHz	18.6°	93.67MHz	28.3°

6. Verification

Physical design verification is accomplished by Design Rule Checking (DRC) and Layout versus Schematics (LVS). DRC verifies that the layout does not violate the manufacturing rules. LVS verifies that the physical layout logically matches the schematic in the number of terminals, components, component sizes and interconnection etc. After the DRC is passed, the layout is extracted and then LVS. After design and layout verification, the analog extracted schematic is created for simulating the circuit performance with parasitics.

6.1 DRC

DRC was performed on the individual level before running on the entire chip. The following figure shows that DRC is passed on the top level, which means that the entire chip does not violate the manufacturing rules and it is ready for next step, extraction.

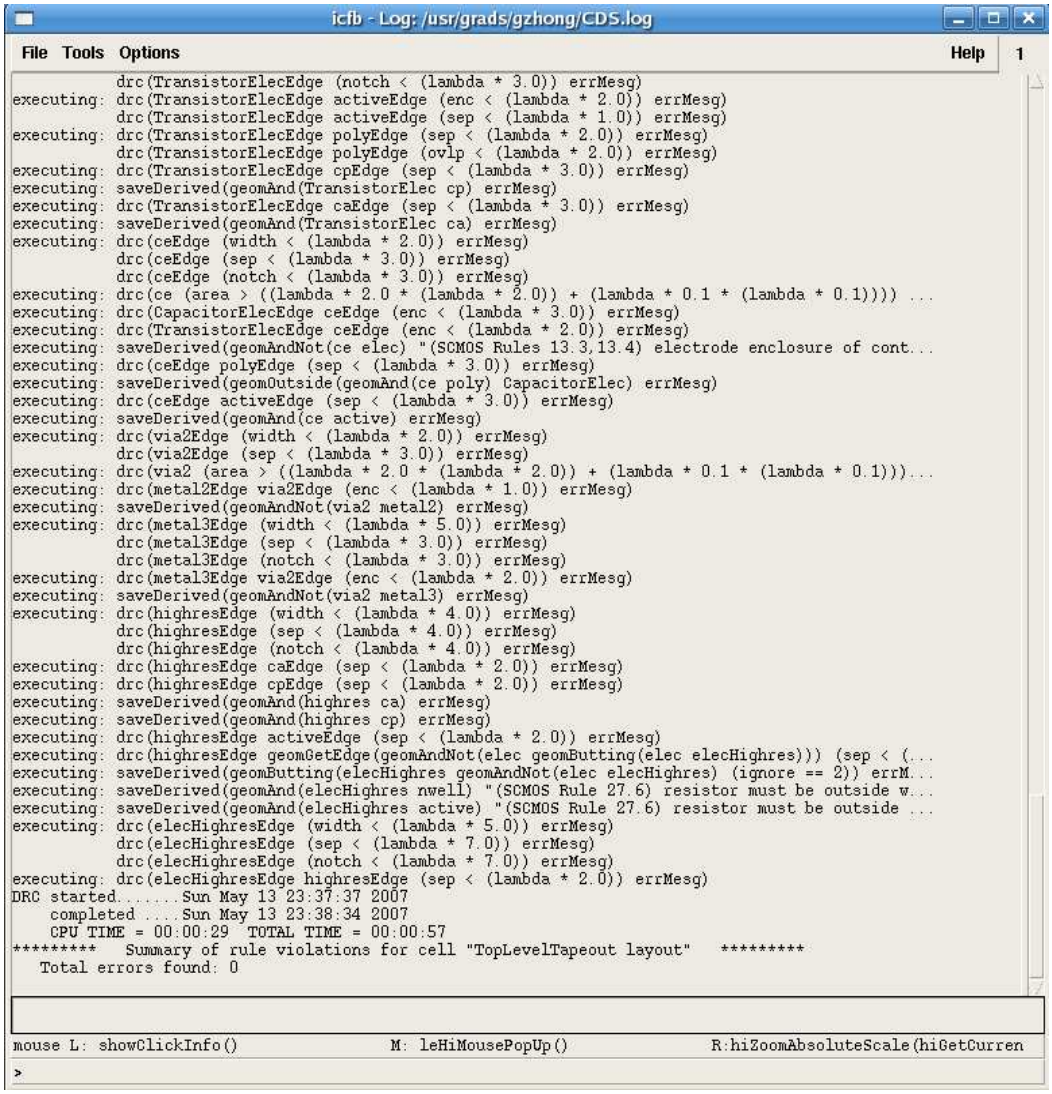

Figure 6.1: Message of "Design Rule Check"

6.2 Extract

Extraction was performed right after DRC and once the layout is extracted, it is ready for LVS.

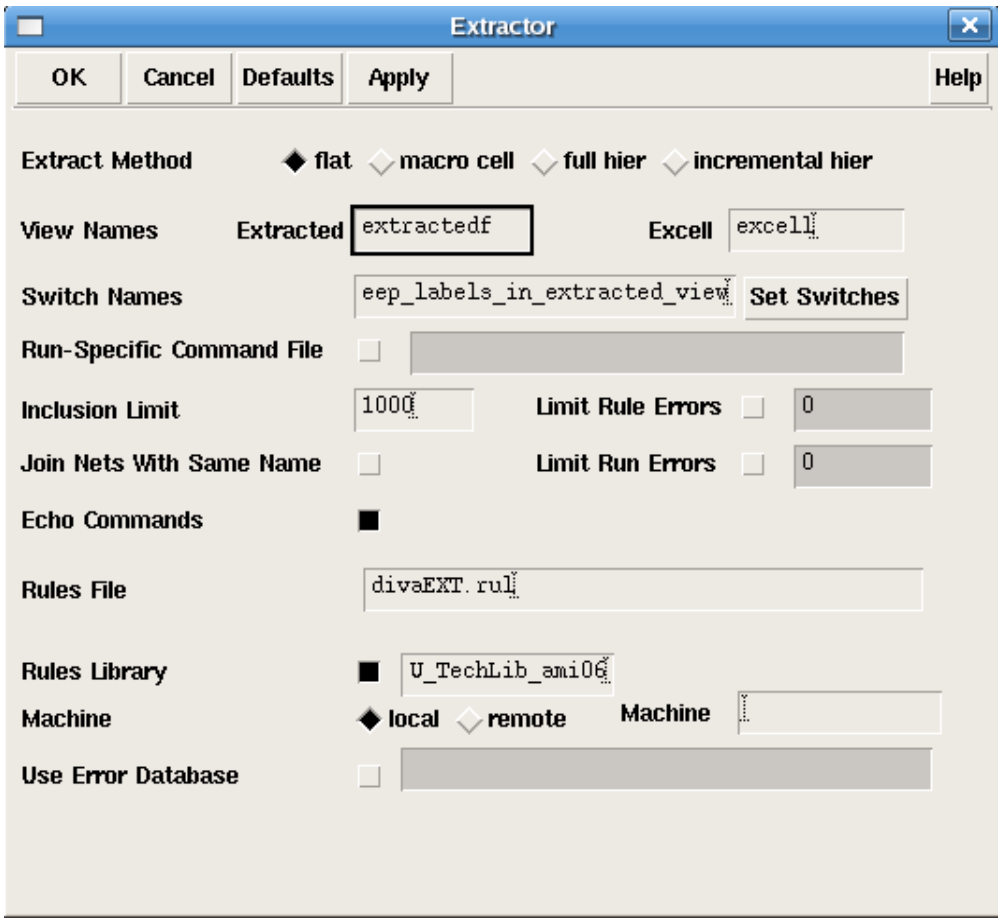

Figure 6.2: Extractor

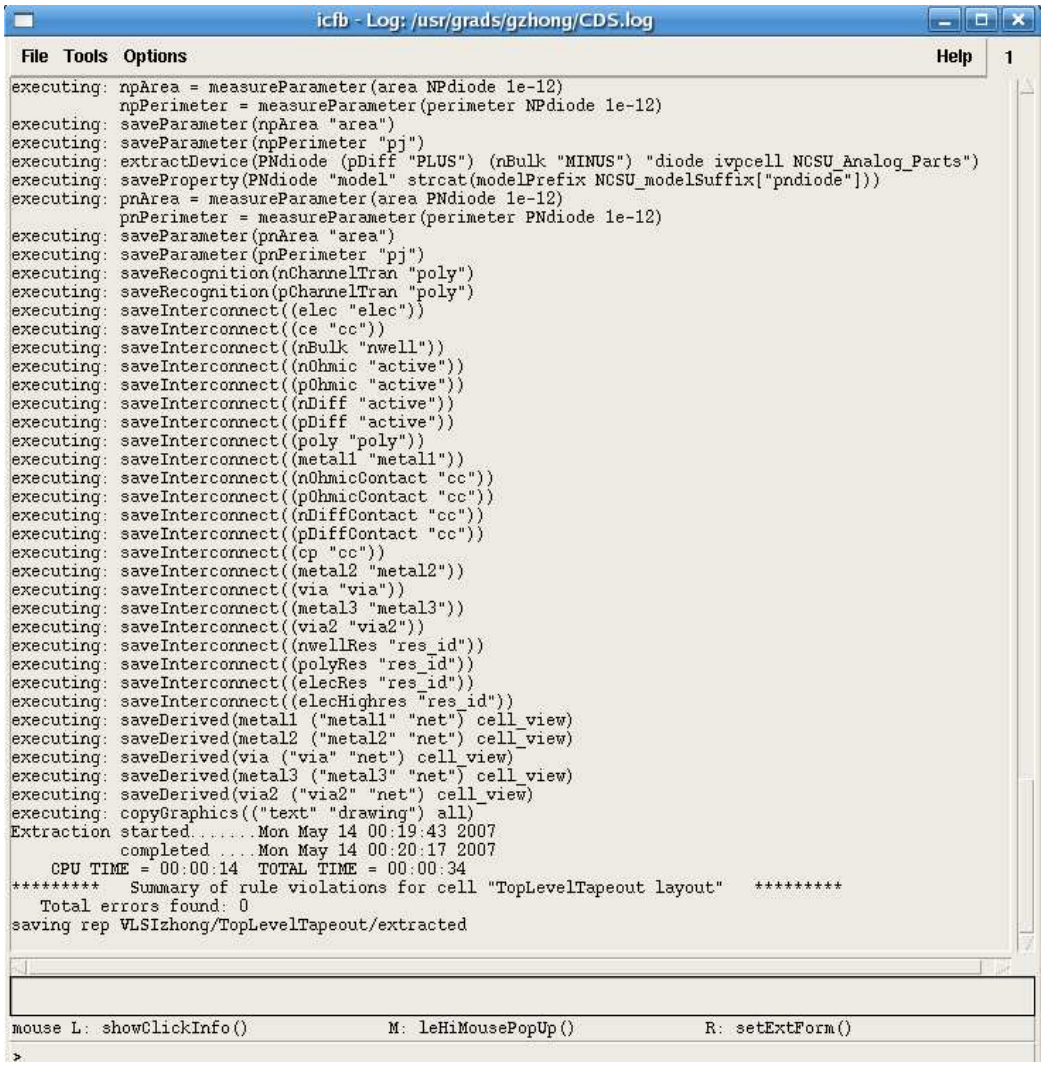

Figure 6.3: Message of “Extraction complete”

6.3 LVS

LVS verifies that the physical layout logically matches the schematic in the number of terminals, components, component sizes and interconnection etc. The following figures show that LVS is passed.

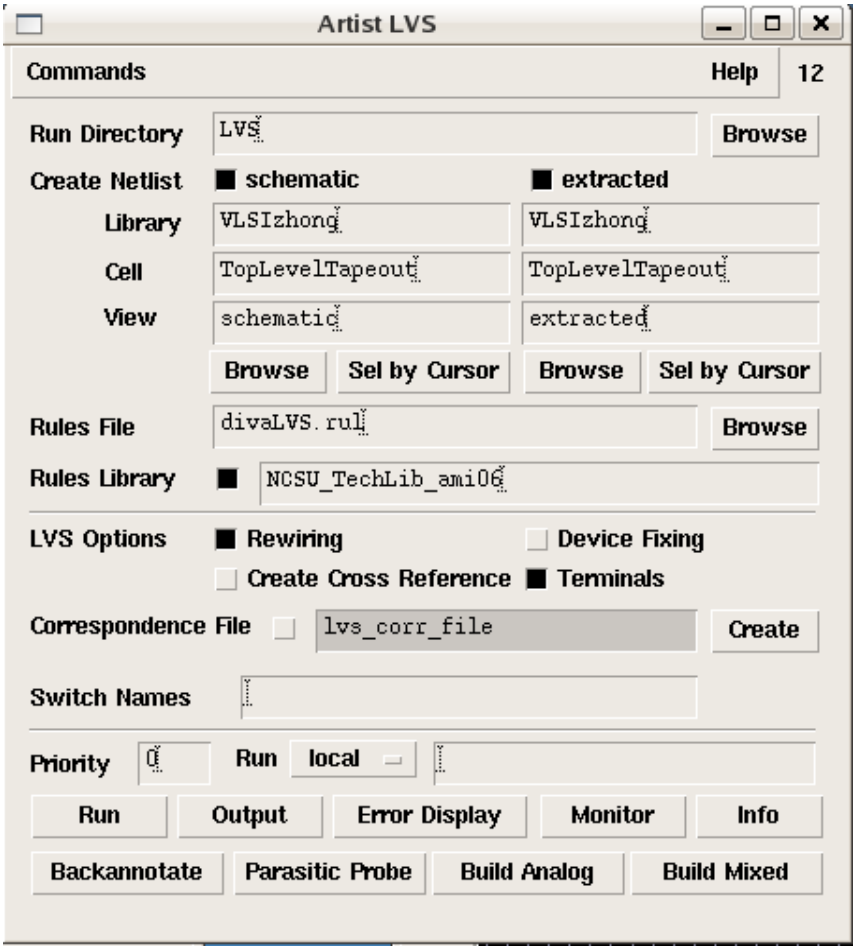

Figure 6.4: Artist LVS

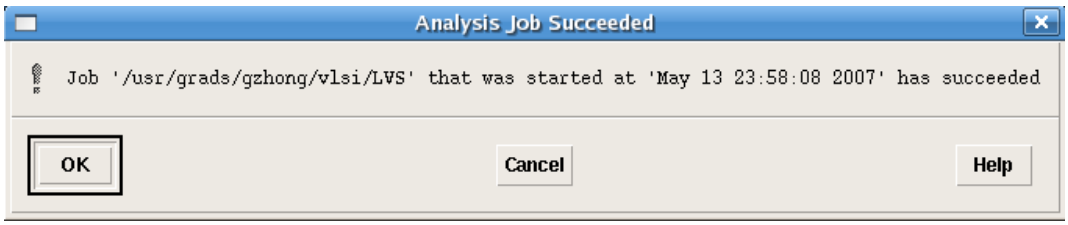

Figure 6.5: Message of "Analysis Job Succeeded"

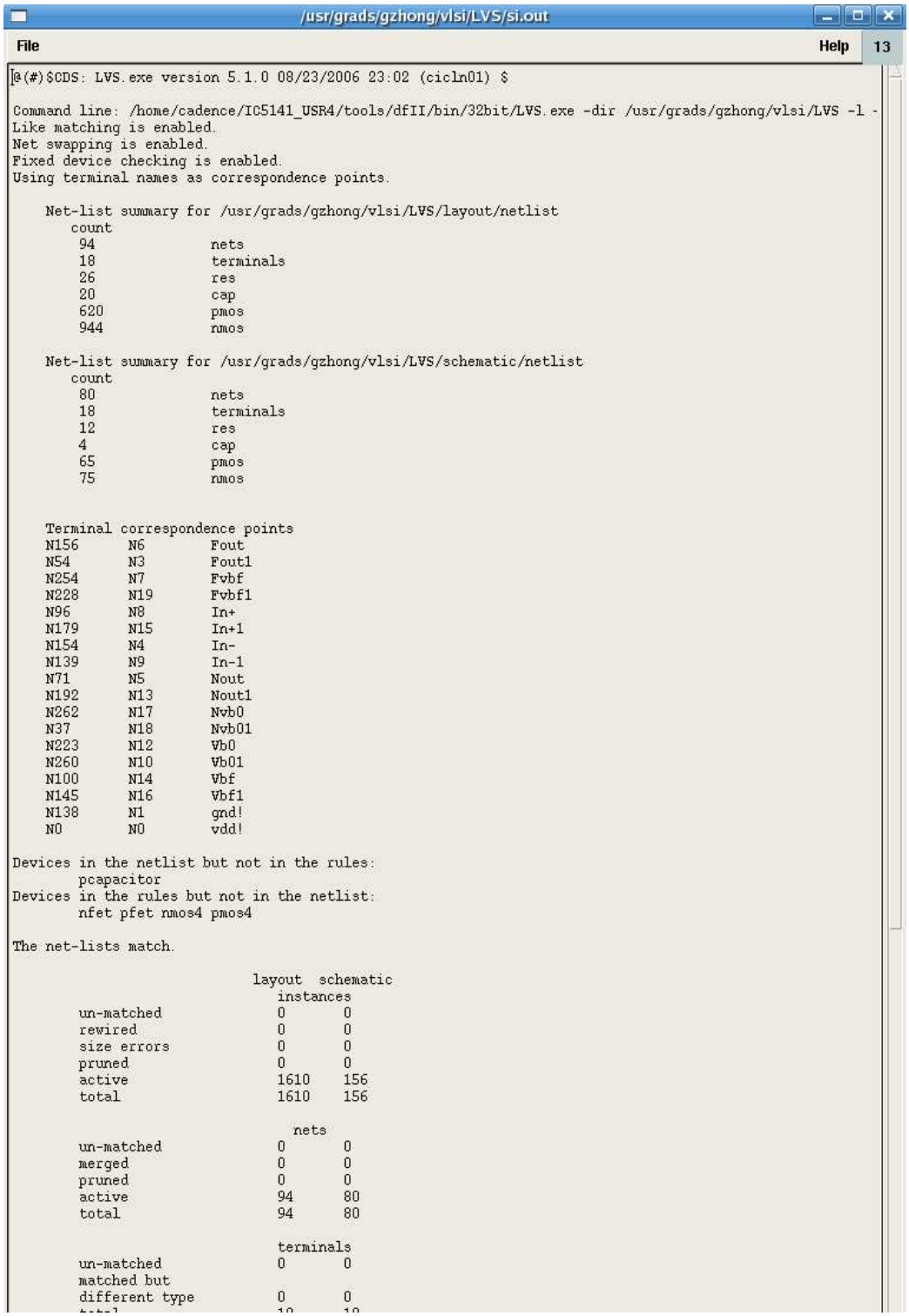

Figure 6.6: Message of “Net-lists match”

Part III

7. Experimental Testing

To measure the noise, a sine wave can be applied to the circuit under test (CUT). The output of the CUT is then amplified and measured by a spectrum analyzer. In such measurement setup, a sine wave source is required. In this setup, radiated signals can introduce error by coupling into the test system through the ground loop.

Figure 7.1 shows another measurement scheme for MOSFET noise measurement [2]. In this setup, no external input signal is needed to apply to the CUT. The noise of the Op-Amp is directly amplified and measured. The CUT can then be placed into a metal box to reduce the coupling of the external radiated signals. This setup is able to achieve a bandwidth from 100 KHz up to 200 MHz, which is necessary to fully characterize the performance the low noise Op-Amps in the range of interested frequency. In this setup, the designed Op-Amps are in unity gain configuration [3]. The noises are amplified by the low noise transimpedance amplifier and then measured by a network/spectrum analyzer such as HP4195A. The additional gain stage in Figure 7.1 is optional. A capacitor is used to decouple the output current of the Op-Amp from the input of the low noise amplifiers. The transfer function defined from the positive input of the Op-Amp to the input of the HP4195A can be measured by applying a reference signal from HP4195A through switch S2 to the positive input of the Op-Amp. The input referred noise spectral density can be obtained by dividing the spectral density of measured output noise by the transfer function. The DUT shares the same inputs. S3 controls which output to be measured. Figure 7.2 shows the schematic of the low noise transimpedance amplifier [2]. Device Q_p is a BFT93 low noise PNP transistor, and Q1 to Q4 are NE856 low noise NPN transistors.

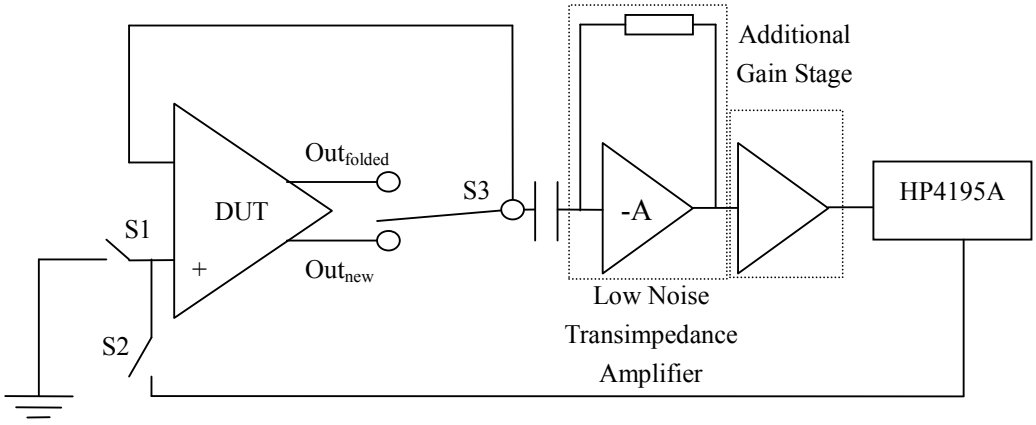

Figure 7.1: Measurement scheme for MOSFET noise measurement

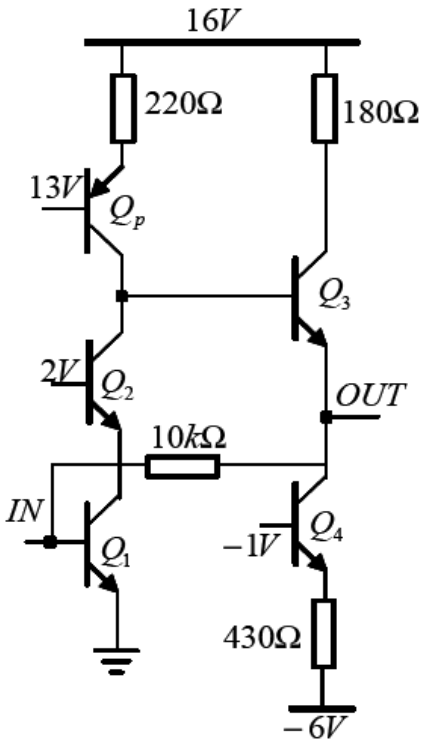

Figure 7.2: Schematic of the low noise transimpedance amplifier

In the tape-out design, all the bias current is internal for the Op-Amps. The bias voltages for the Op-Amps are externally tunable. In such a design, the parameters of the Op-Amps can be tuned to desired values for performance comparison. In the post

layout simulation, we have known that the external bias is necessary because of the parasitics. The bias voltage needs to be tuned to achieve reasonable gain.

The requirement for the testing PCB would be including a 5 Volts working voltage and two bias voltages. Recommended values for these two bias voltages would be 2.45V for the Folded-Cascode structure, and 4.64V for the new structure Op-Amp. The PCB should be also including all the other necessary voltage/current sources, for example, reference voltages for the low noise transimpedance amplifier.

Figure 7.3 shows the simplified schematic for the PCB testing board.

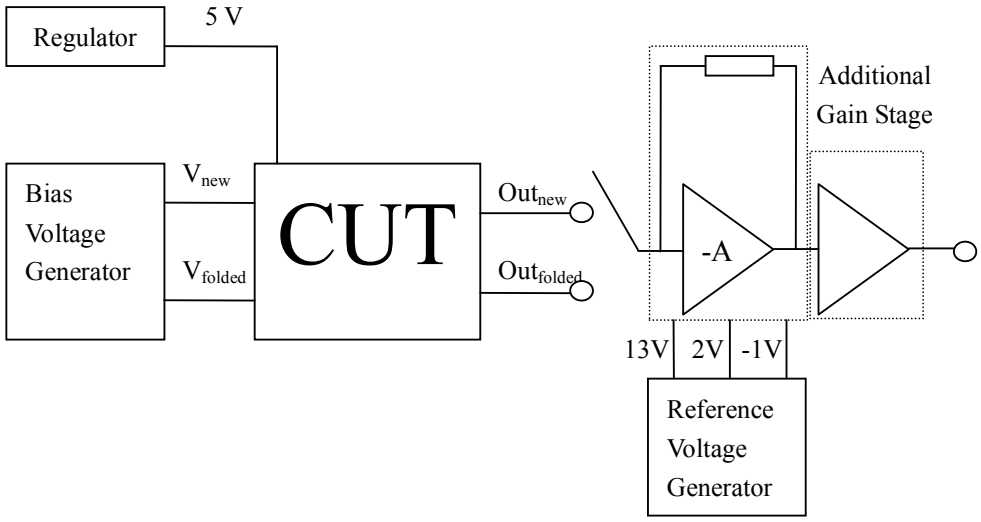

Figure 7.3: Simplified schematic for the PCB testing board

The Op-Amp should show some correct amplification behavior with some gain when in inverting configuration. Figure 7.4 shows the sine wave input setup. If one chooses 1 KHz sine wave as the input signal, R1=2kΩ and R2=100KΩ, then the oscilloscope should show a gain of 50 and a phase difference of 180° between the input and the output.

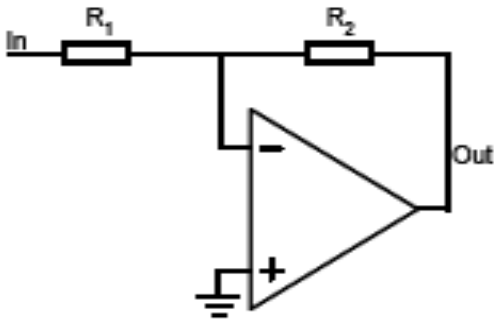

Figure 7.4: Sine wave input setup [1]

The AC gain measurement setup is shown in Figure 7.5. The voltage at the point A is too small to be directly measured. However, the value of V_A can be obtained by V_B through $V_A = V_B(\frac{R_0}{R_0 + R_3})$. AC gain at a given frequency is $A = \frac{Out}{V_A}$.

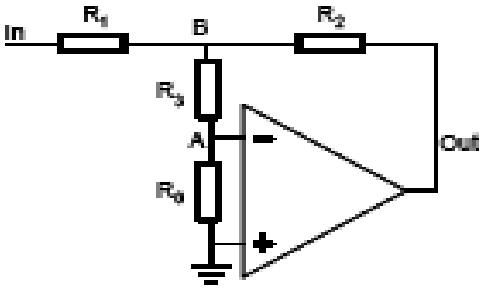

Figure 7.5: AC gain measurement setup [1]

Part IV

8. Summary and conclusion

Two Op-Amps including a new structure and a Folded-Cascode structure are designed, laid out, and simulated based on the 0.5 micron CMOS process. While the literature emphasizes the reduction of flicker noise, the two structures in the project minimized the flicker noise and thermal noise simultaneously. These two Op-Amps are capable of operating in the frequency range of 1-10 MHz. Our results show that the two Op-Amps have comparable performance in simulation.

9. Suggestions for future studies/work

Although the objectives of the project were achieved successfully, there are several improvements can be made in the future work.

1. The width of the input pair of the low noise Op-Amp can be made larger to further decrease the flicker noise.

2. The bias current goes through the input pair can be made larger to further decrease the thermal noise.

3. If performance comparison of the two Op-Amps is not the objective, the gains of these two Op-Amps can be tuned to higher values.

4. The noise model for the simulation in Cadence needs to be added.

10. Biography of the author

Guixiong Zhong was born in Shantou, China and attended primary and secondary school in Shantou, China. He completed his M.S. in Physics from the University of Maine in May 2007. He is currently working towards a Master of Science in Electrical Engineering with a focus in the area of IC design and fabrication at the University of Maine.

Part V

11. Appendices for complete schematics and layout views

Appendix A

Complete schematics

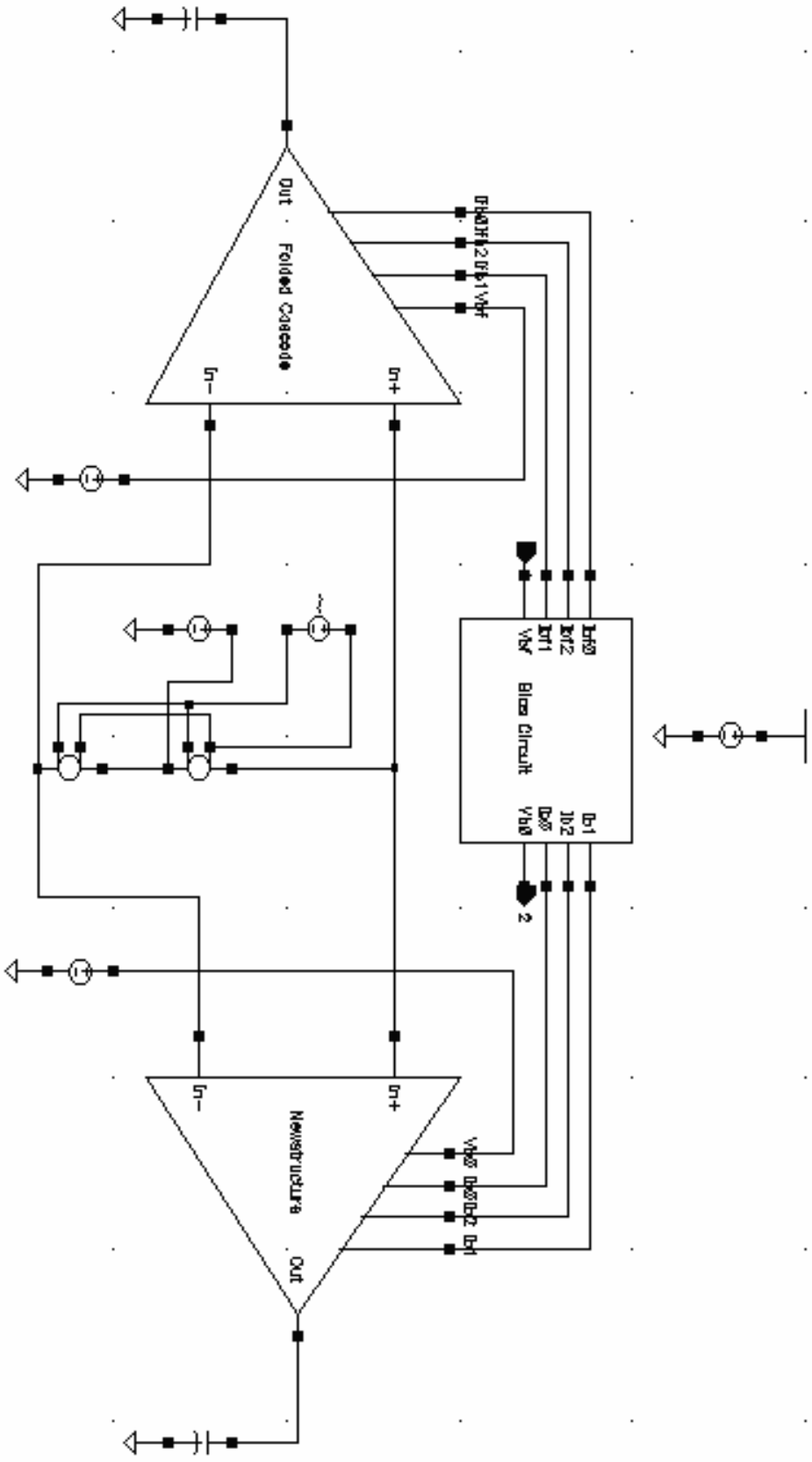

Figure A.1: Test schematic for post layout

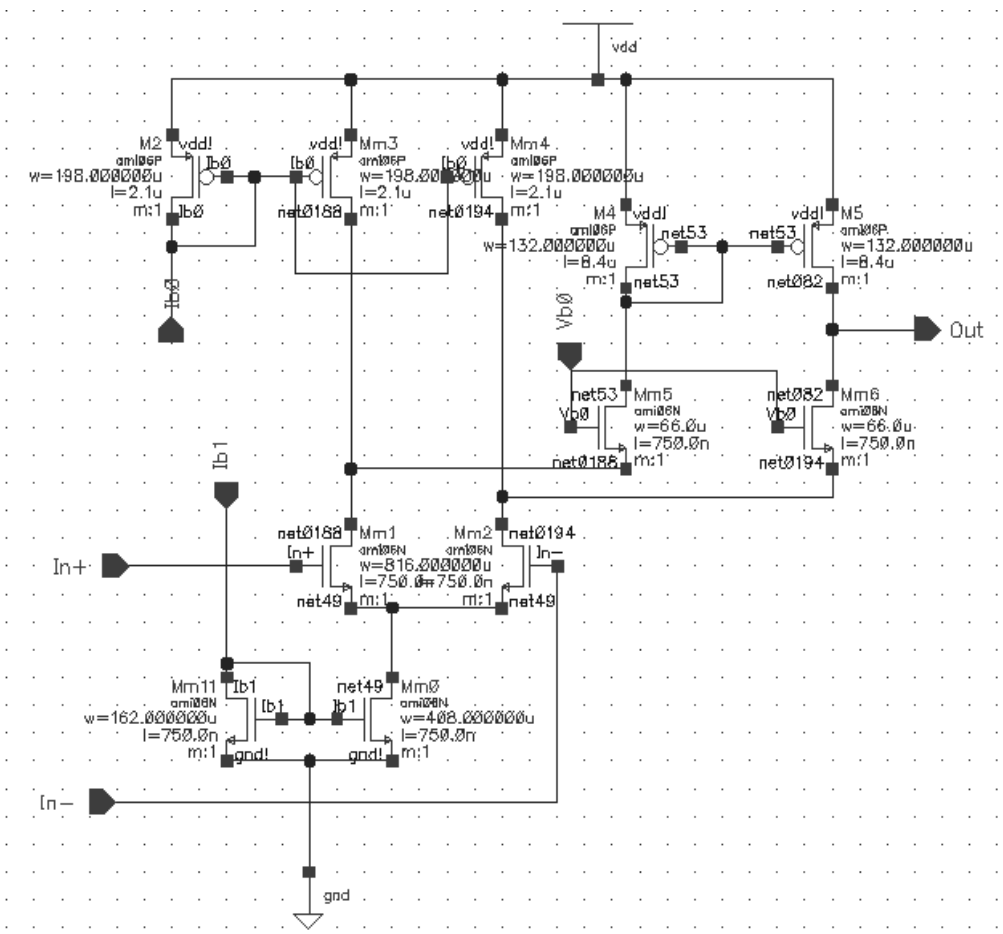

Figure A.2: Schematic of the new structure Op-Amp

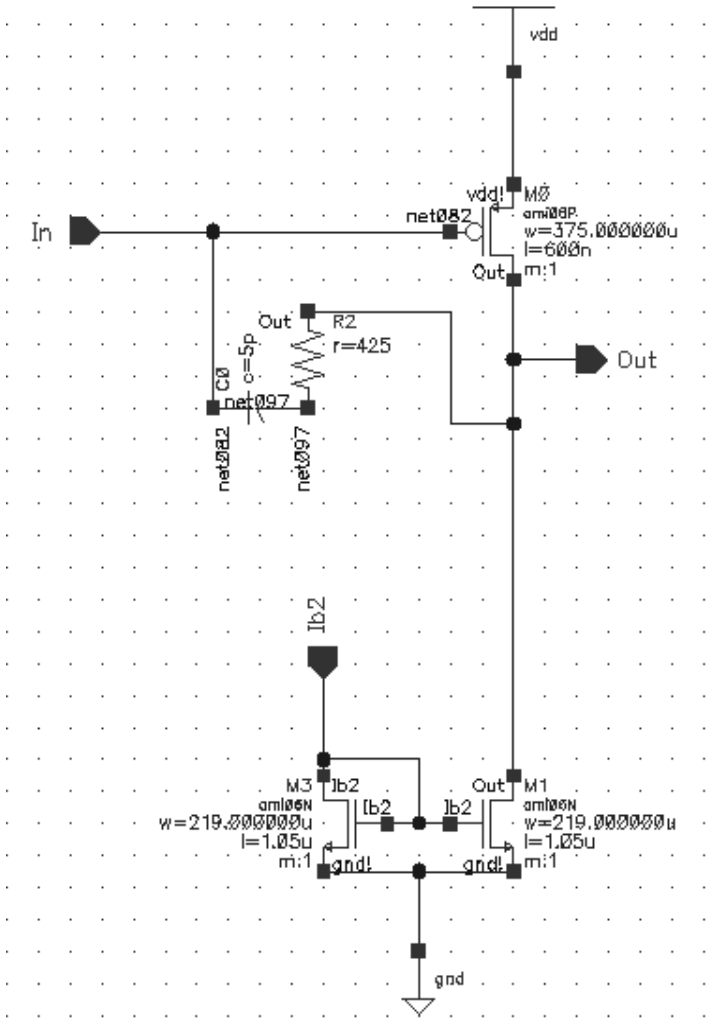

Figure A.3: Schematic for the second stage of the new structure Op-Amp

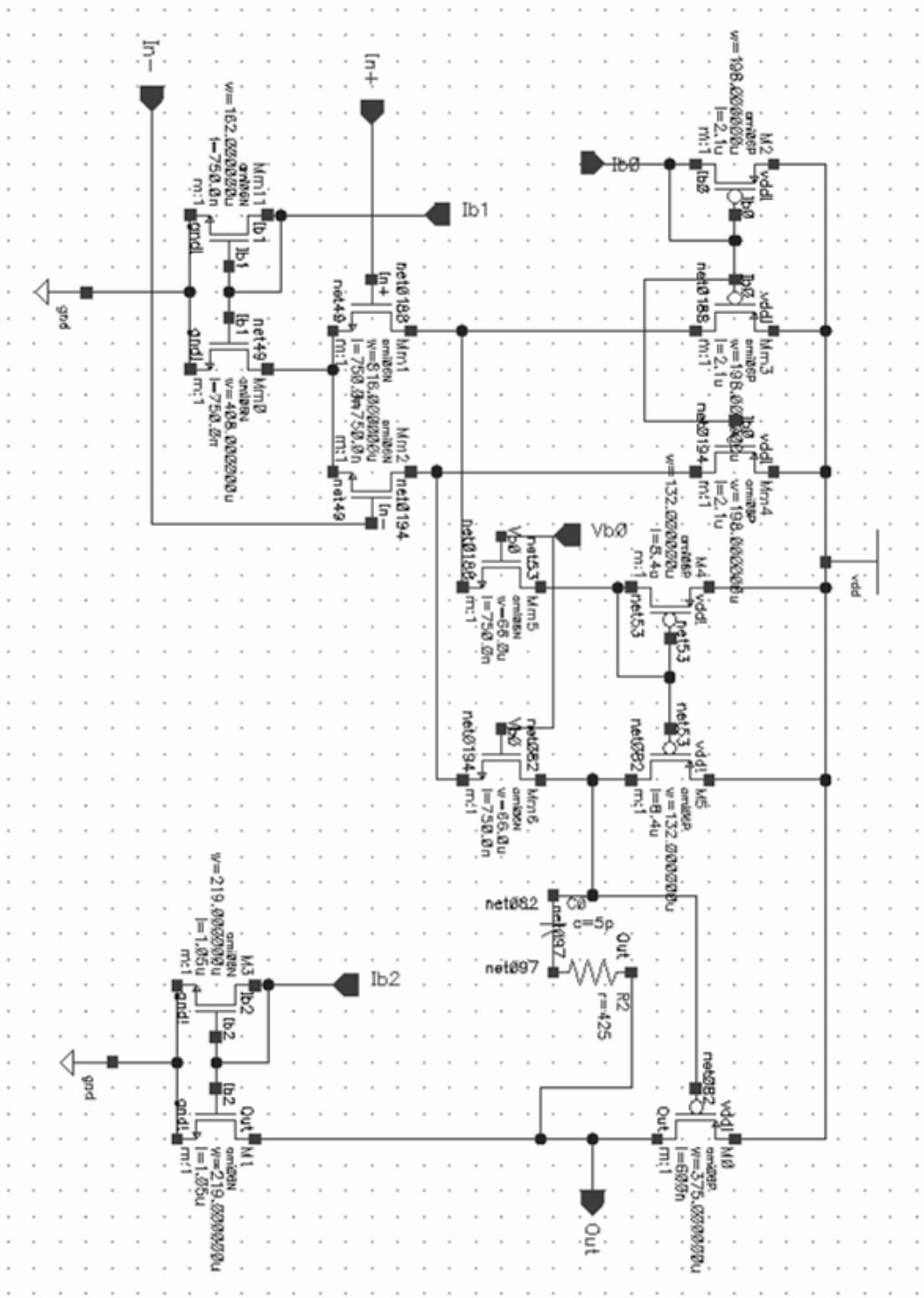

Figure A.4: Schematic of the two stage new structure Op-Amp

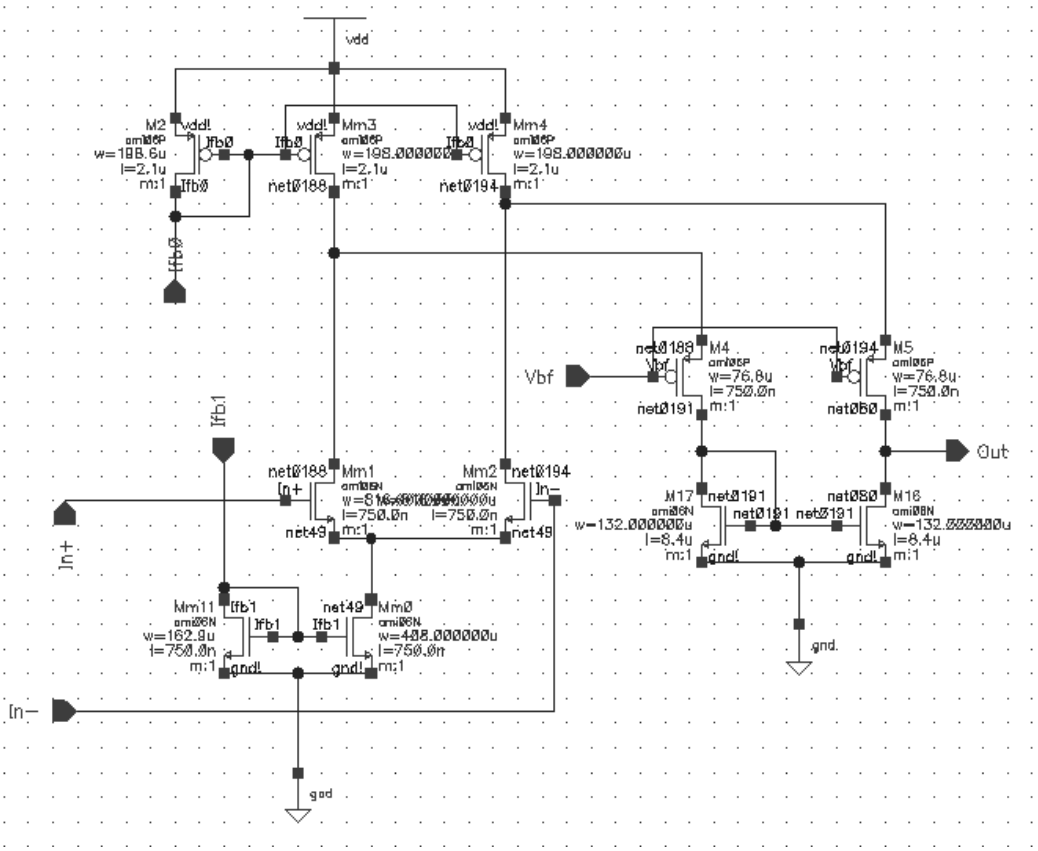

Figure A.5: Schematic of the Folded-Cascode Op-Amp

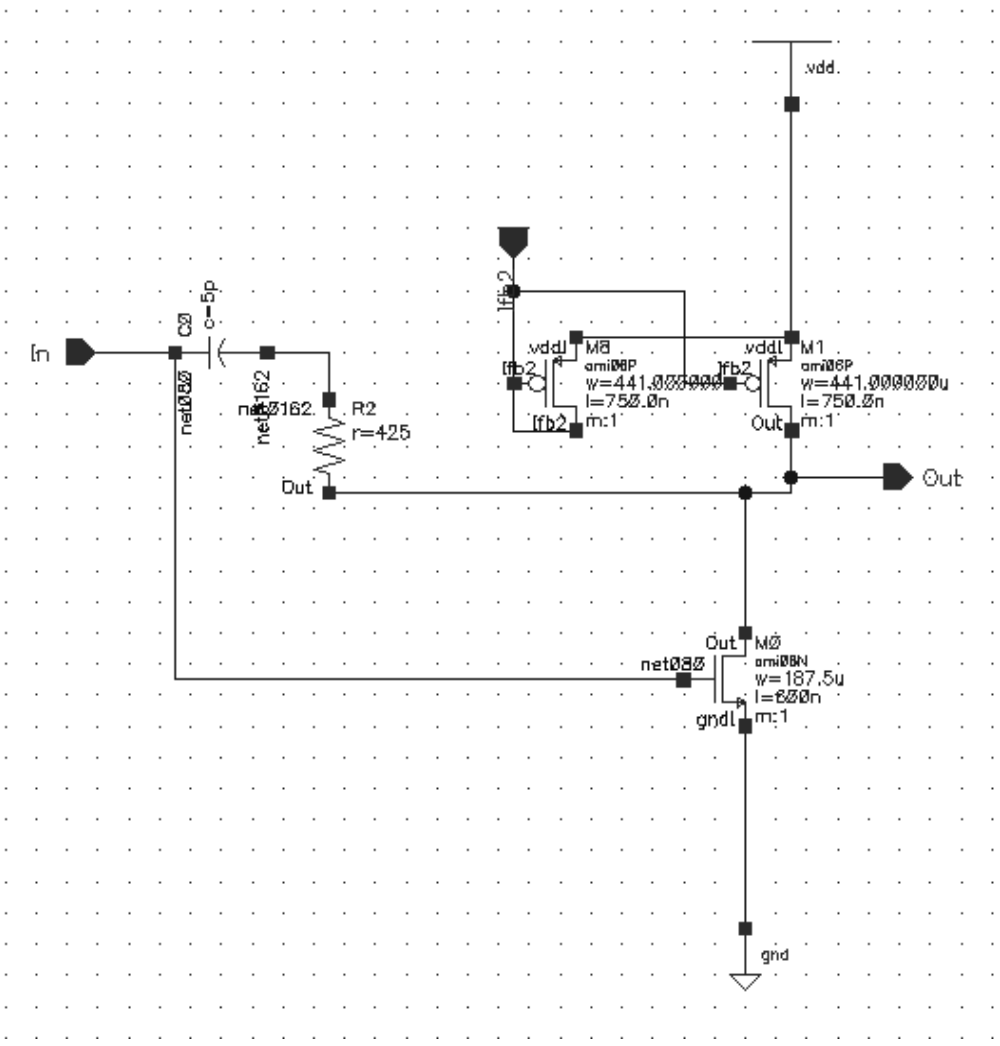

Figure A.6: Schematic for the second stage of the Folded-Cascode Op-Amp

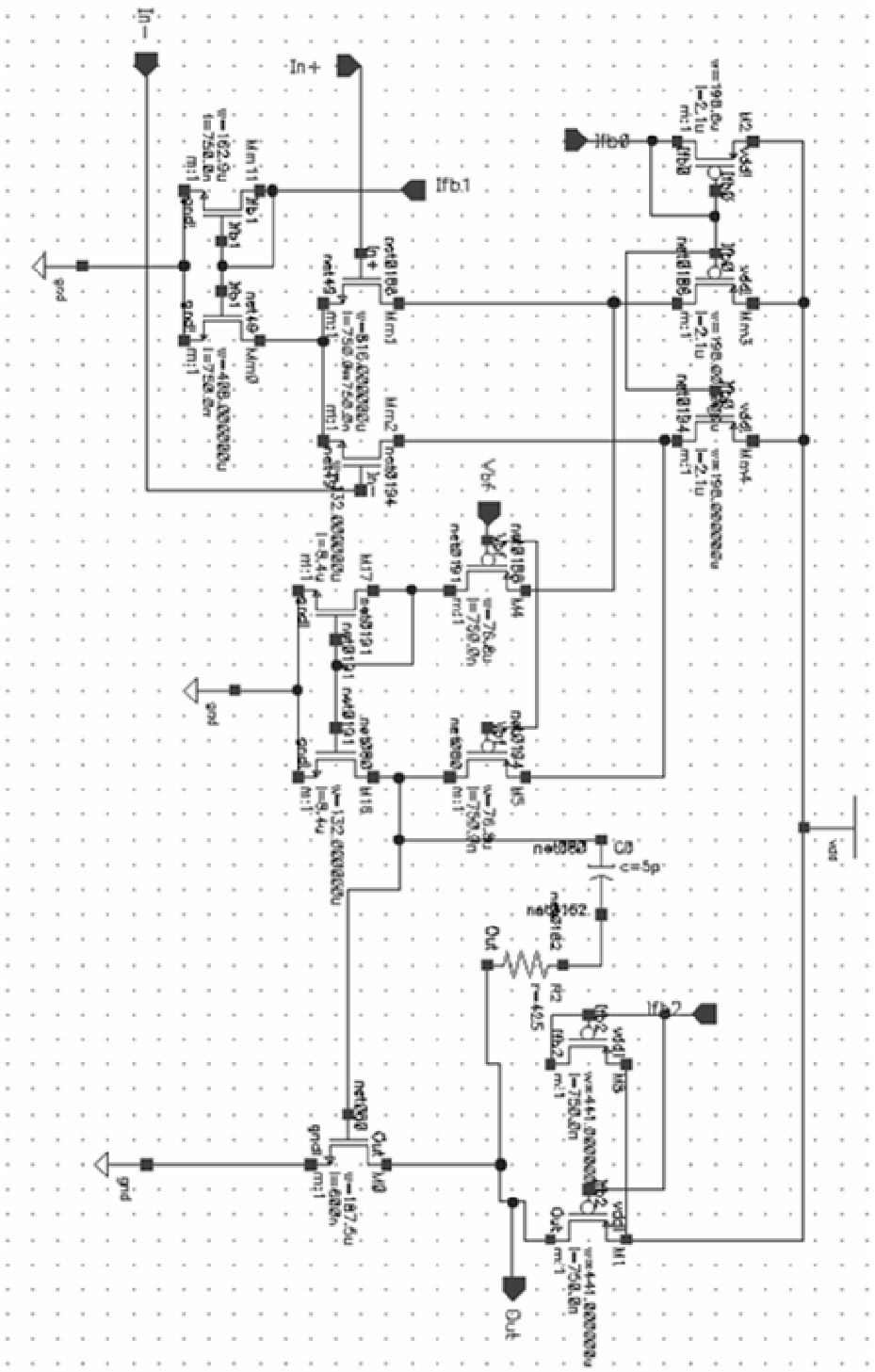

Figure A.7: Schematic of the two stage Folded-Cascode Op-Amp

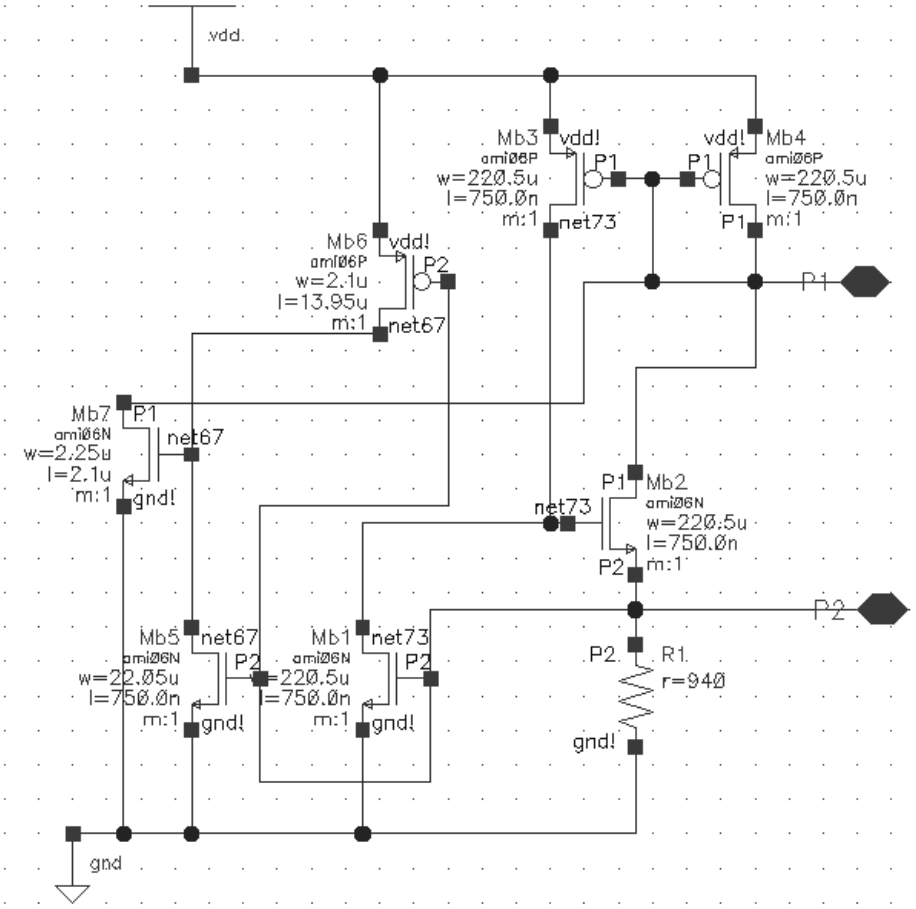

Figure A.8: Schematic of the bias core

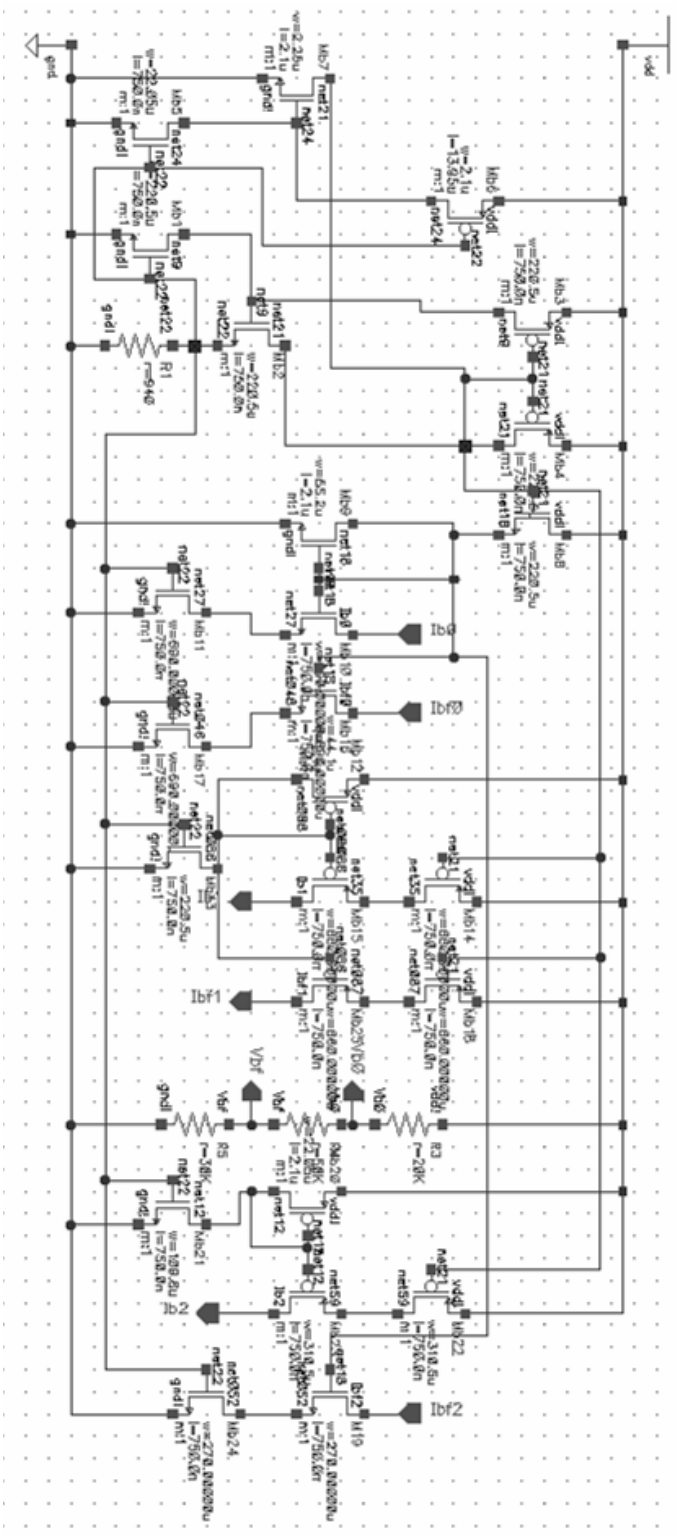

Figure A.9: Schematic of the entire bias circuit

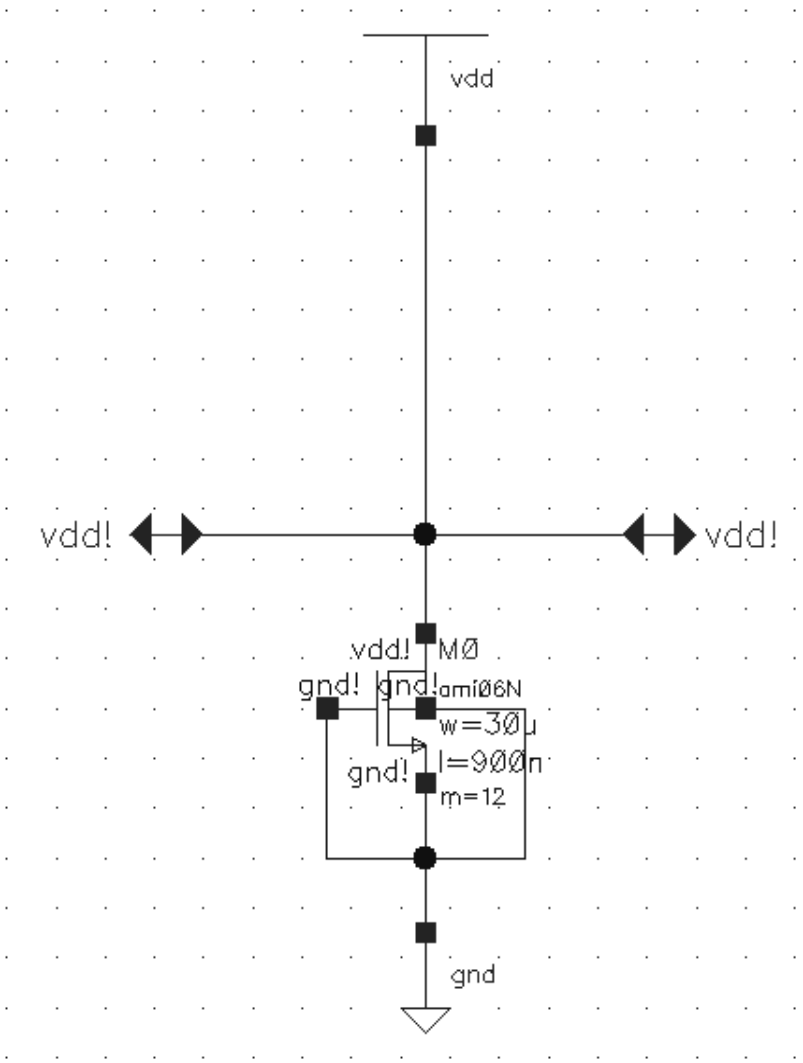

Figure A.10: Schematic of Pad Vdd

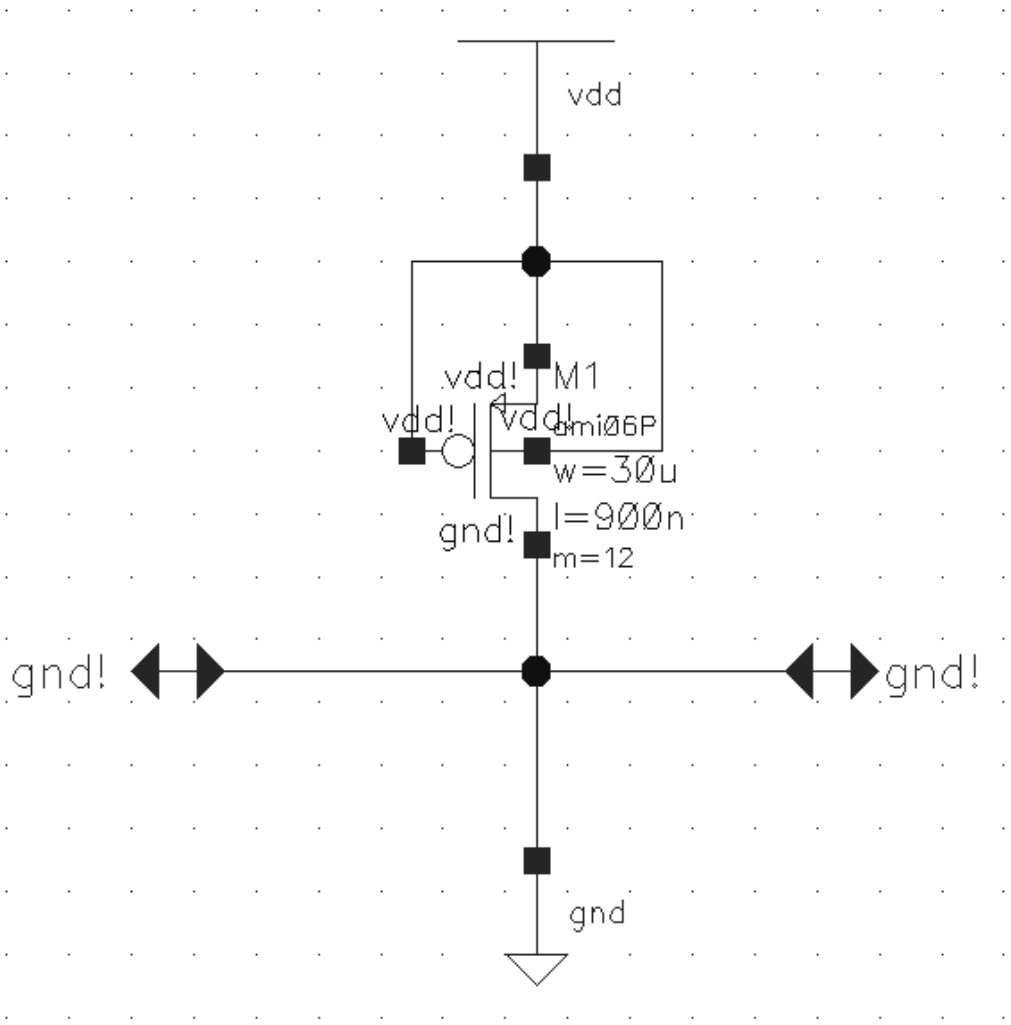

Figure A.11: Schematic of the Pad ground

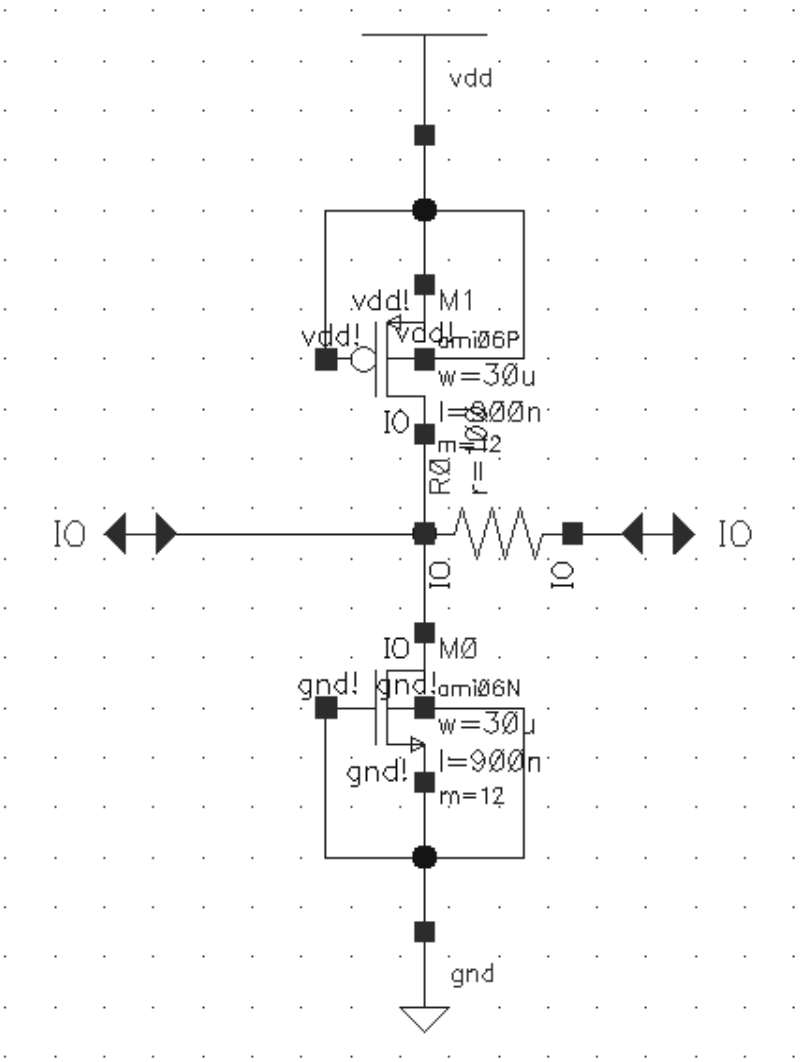

Figure A.12: Schematic of the Pad IO

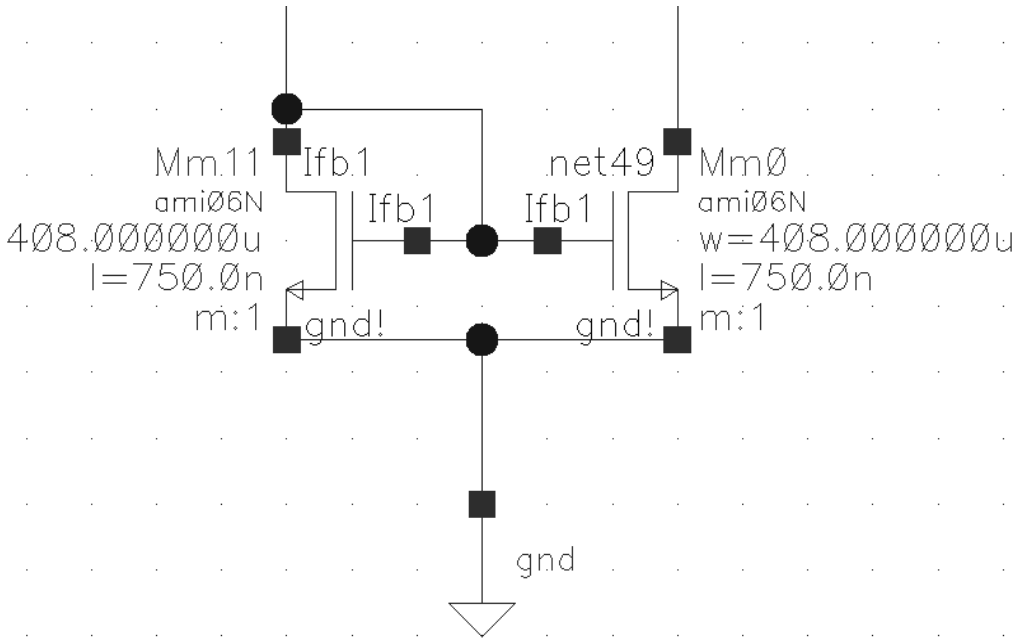

Figure A.13: Schematic of a current mirror

Appendix B

Complete layout views

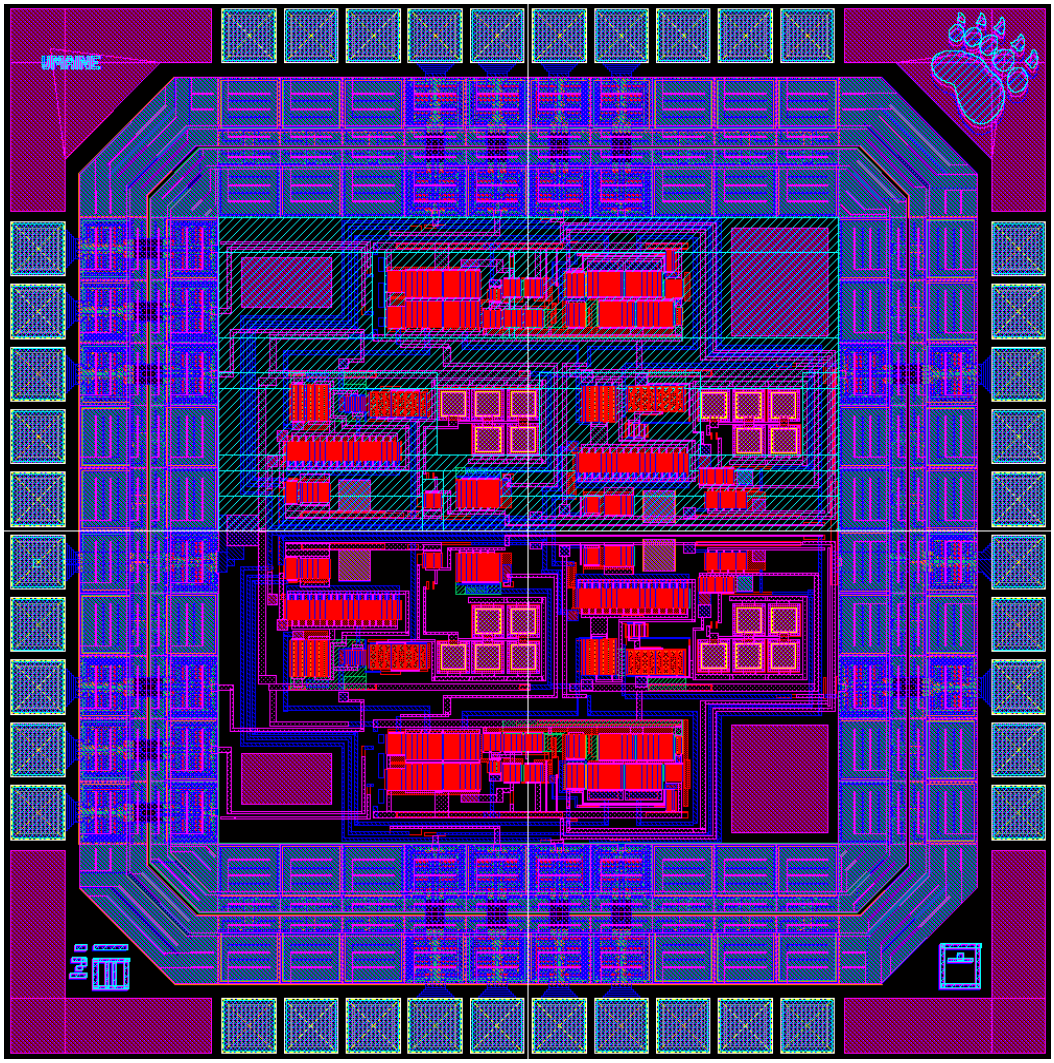

Figure B.1: Layout of the entire chip

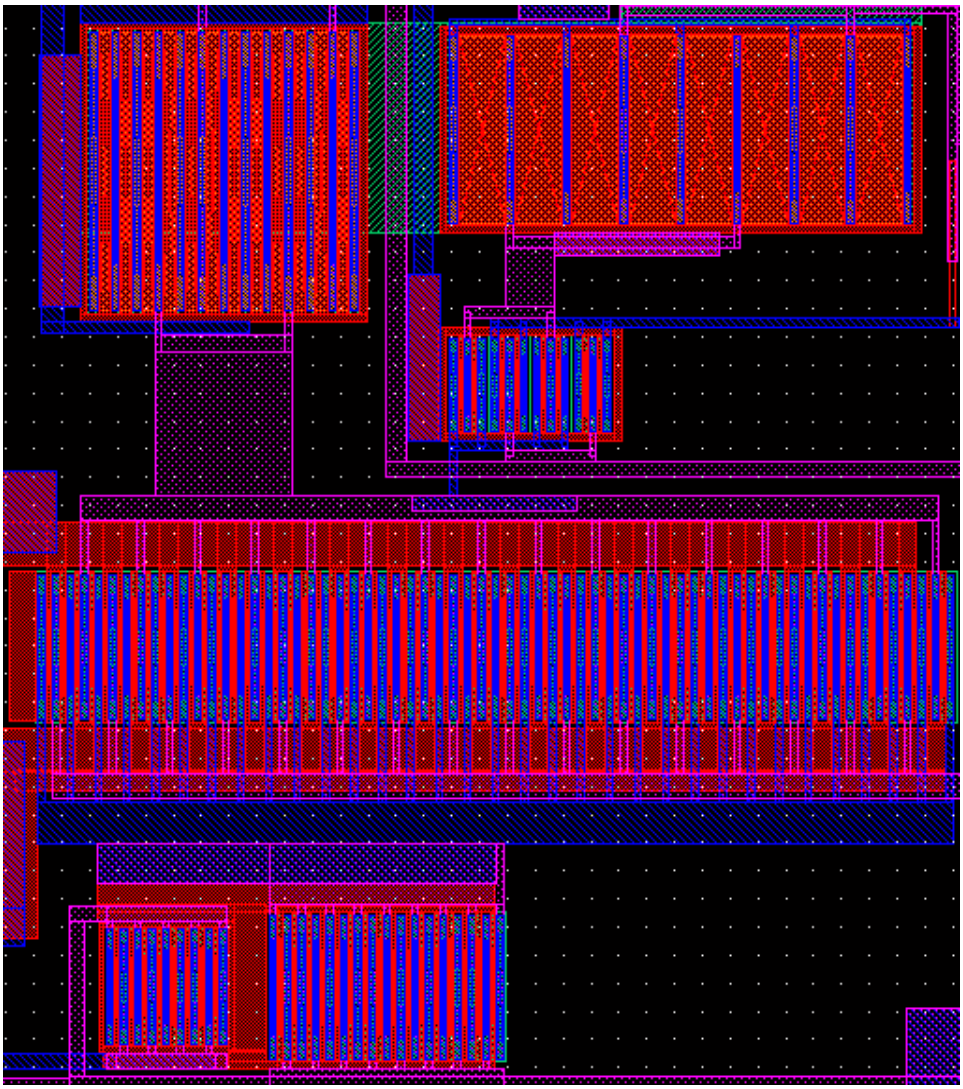

Figure B.2: Layout of the new structure Op-Amp

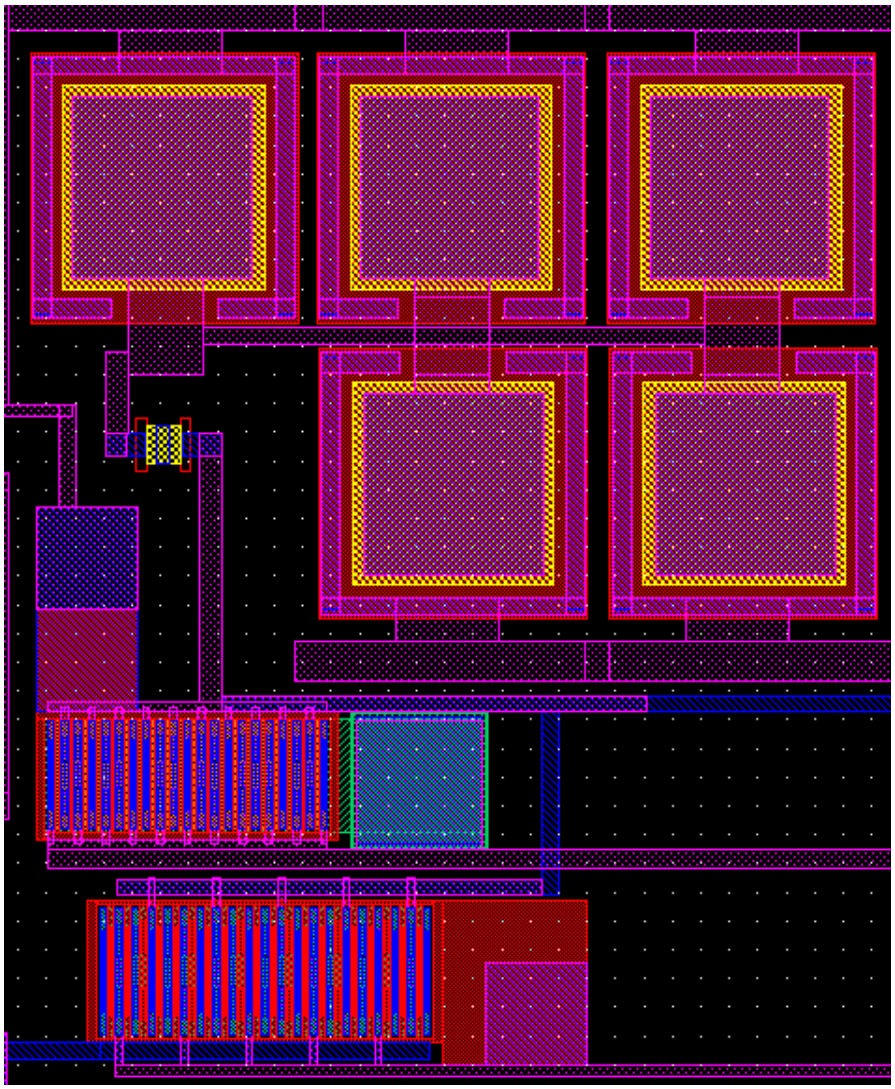

Figure B.3: Layout of the second stage for the new structure Op-Amp

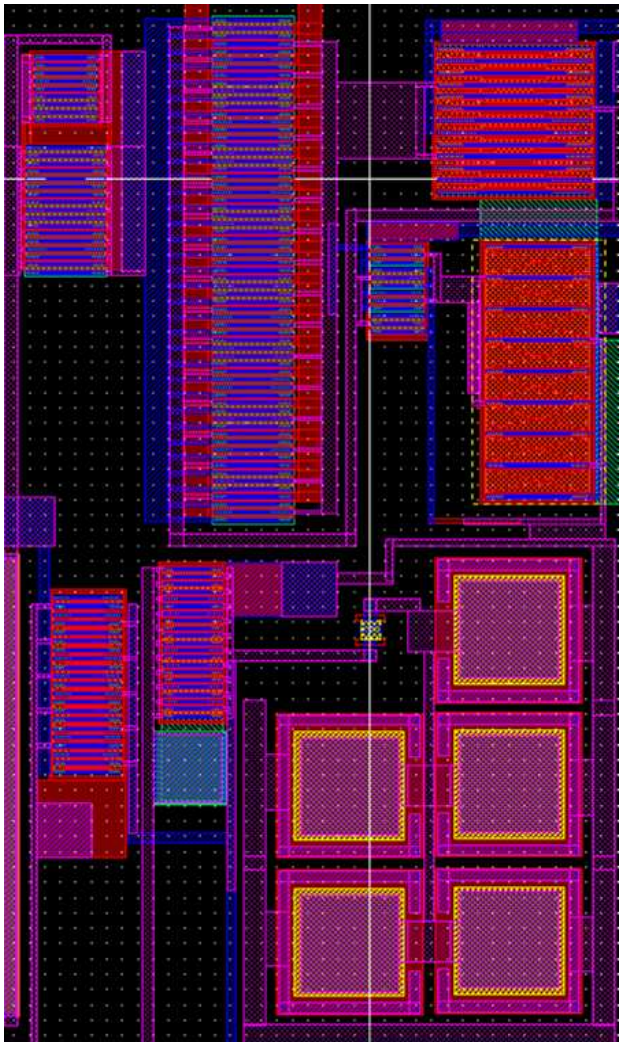

Figure B.4: Layout of two stage new structure Op-Amp

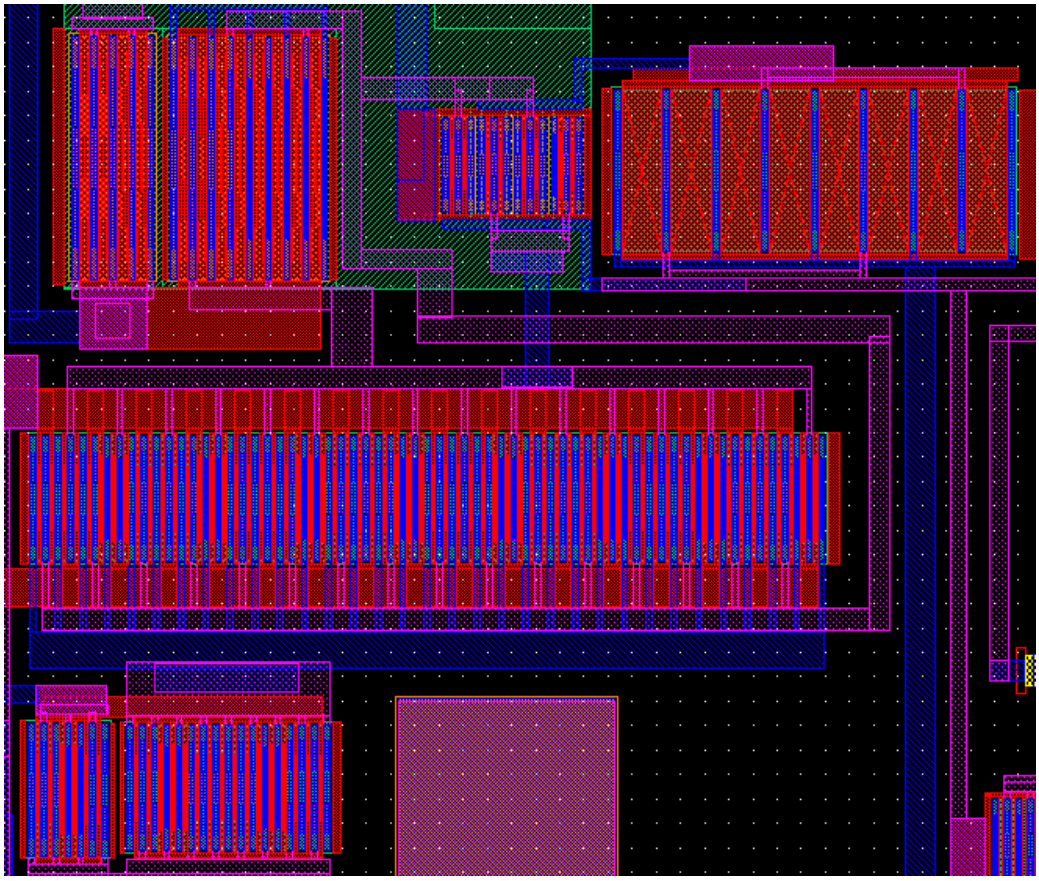

Figure B.5: Layout of Folded-Cascode Op-Amp

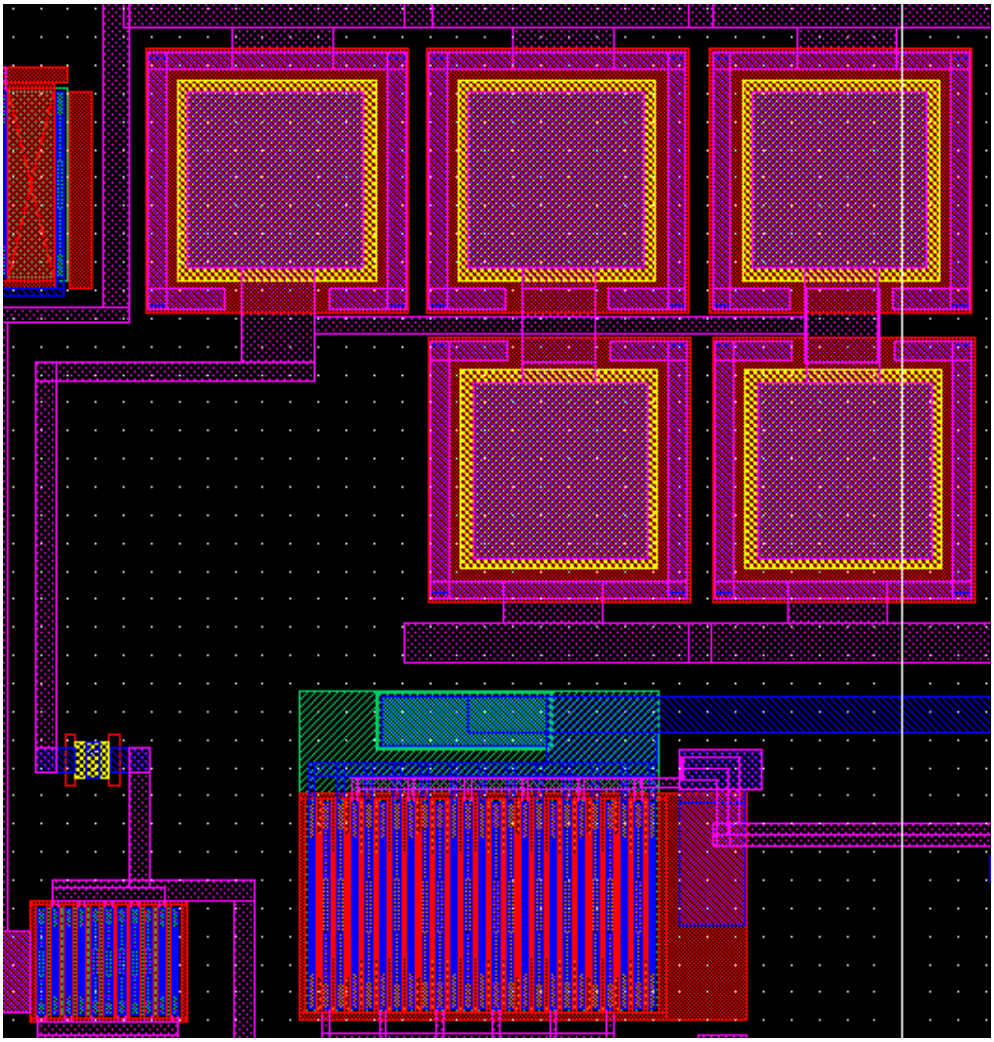

Figure B.6: Layout for the second stage of the Folded-Cascode Op-Amp

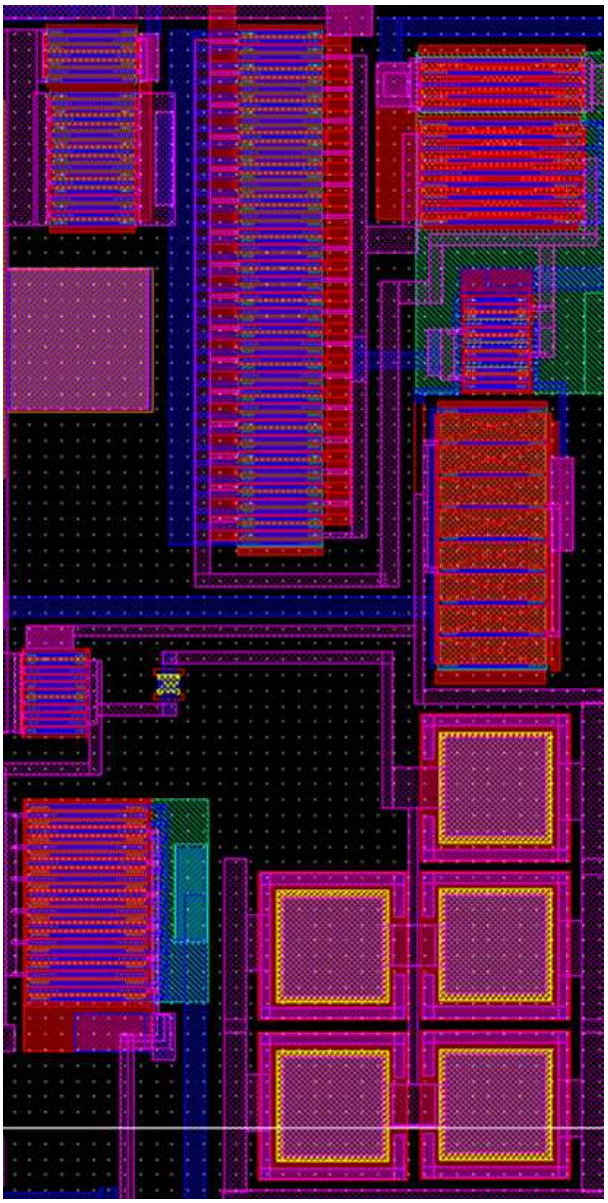

Figure B.7: Layout of Folded-Cascode Op-Amp

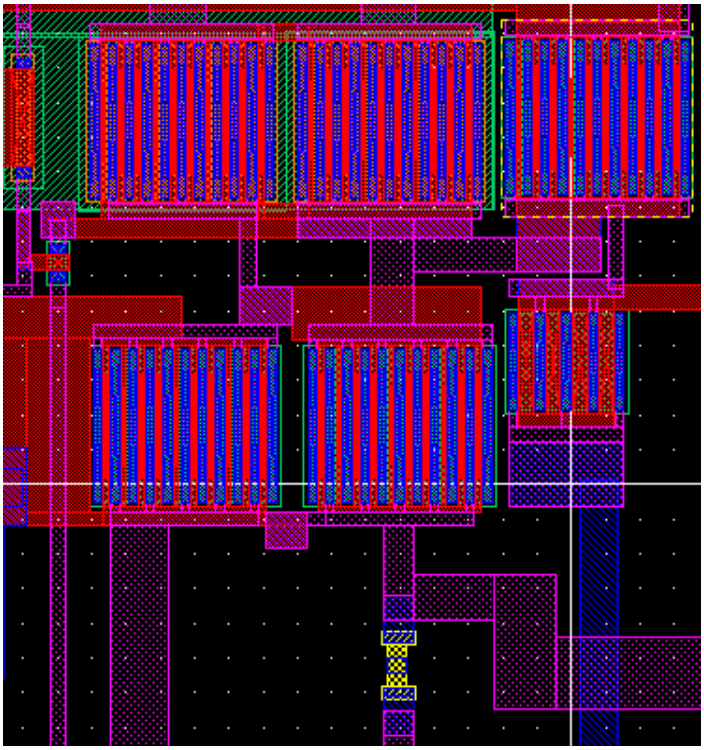

Figure B.8: Layout of the bias core

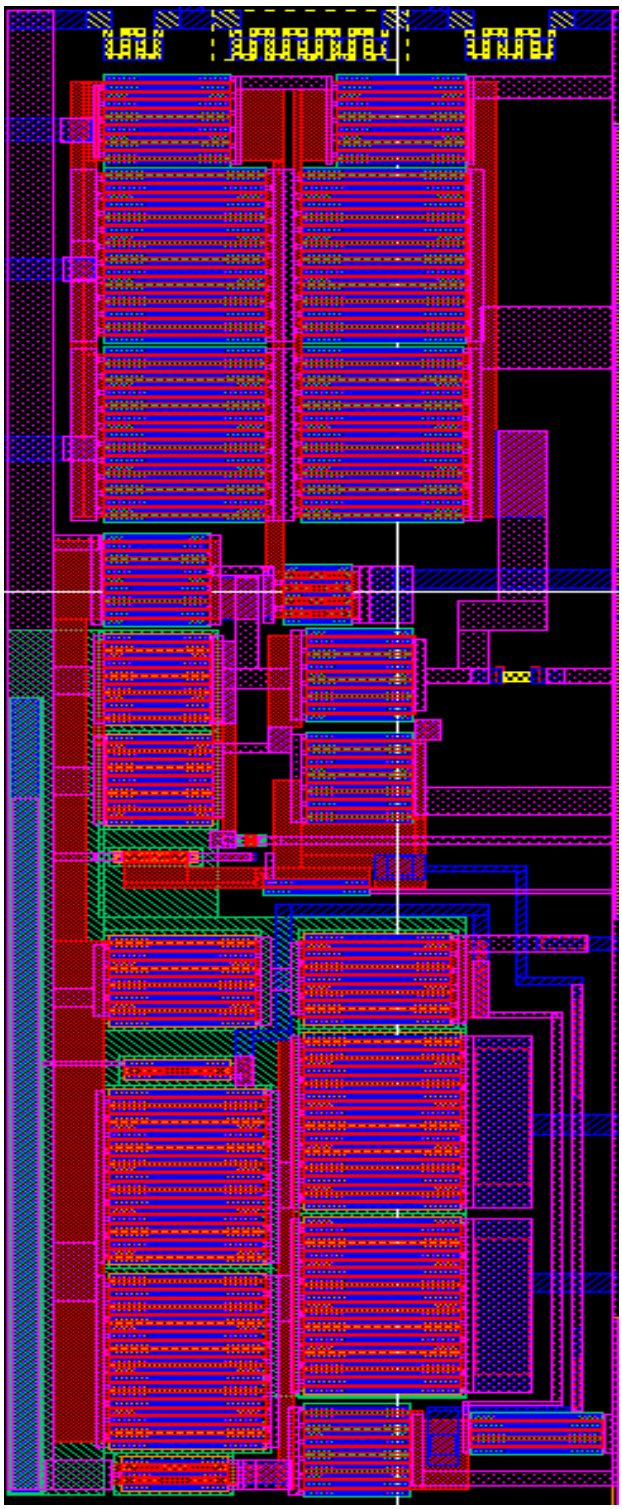

Figure B.9: Layout of the entire bias circuit

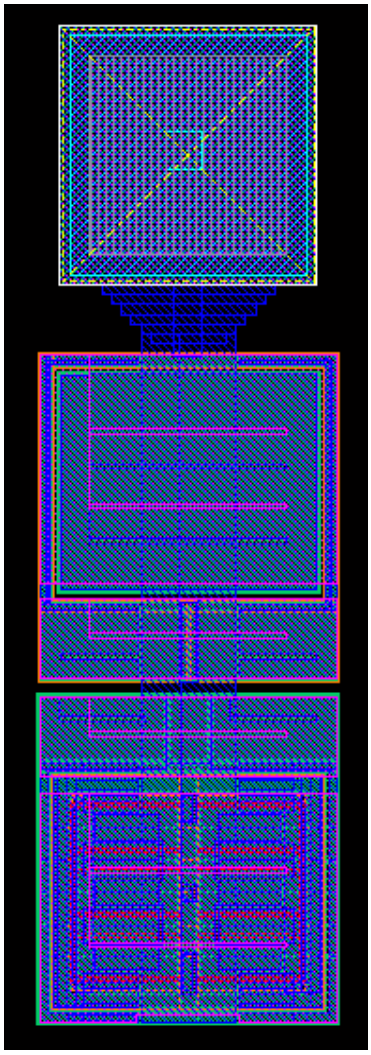

Figure B.10: Layout of Pad Vdd

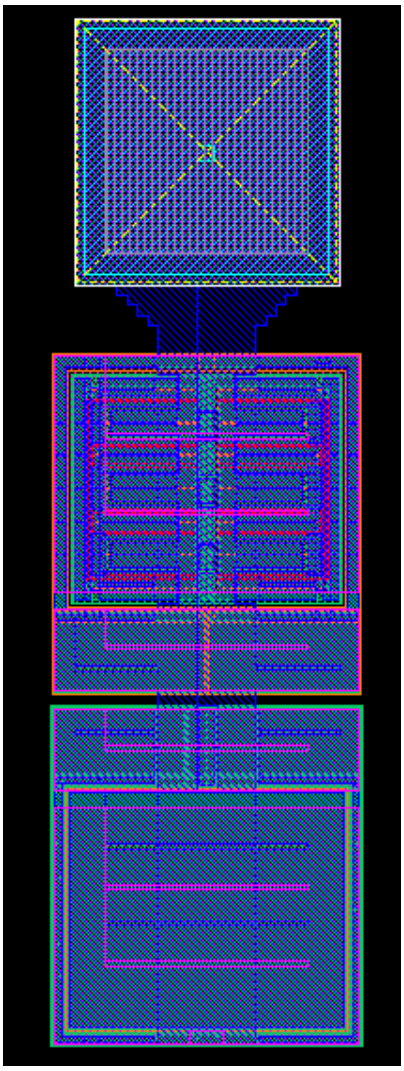

Figure B.11: Layout of Pad ground

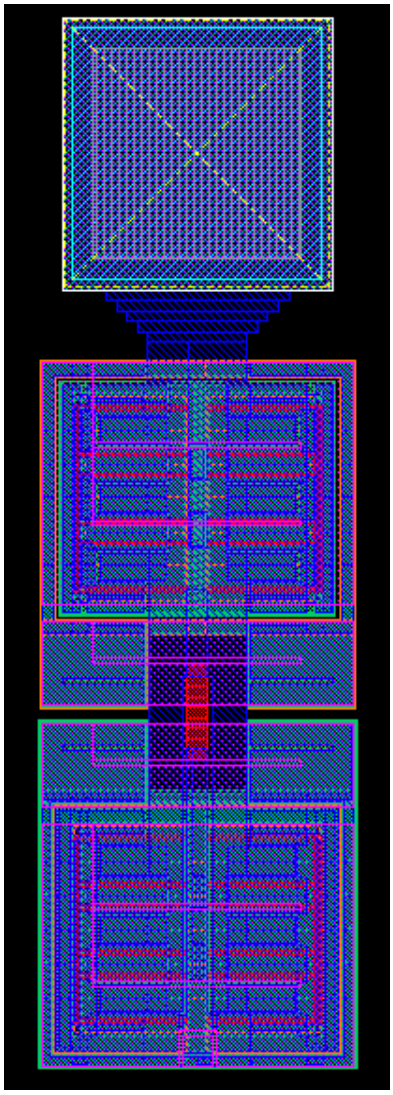

Figure B.12: Layout of the Pad IO

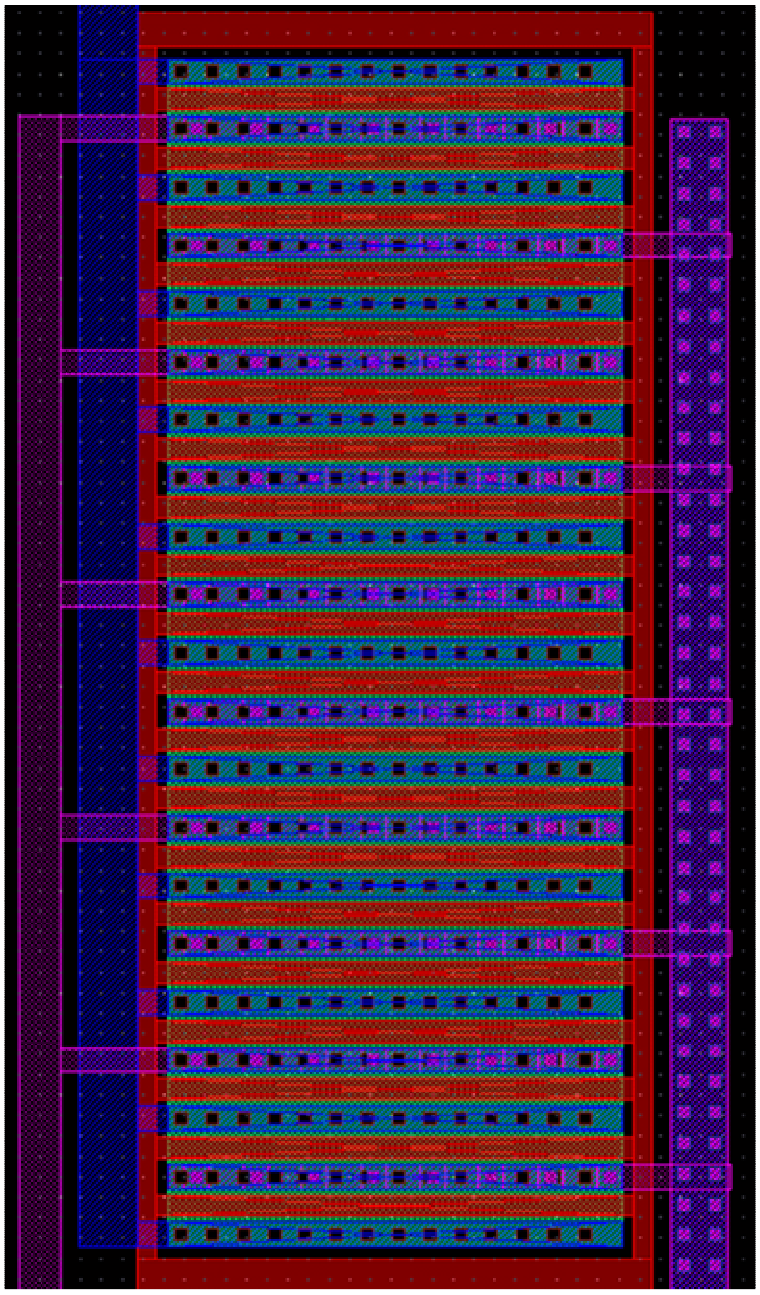

Figure B.13: Layout of a current mirror

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[3] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation. Hoboken, NJ, John Willey, 2005.