An Analog Phase-Locked Loop

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ABSTRACT

This report discusses the design, simulation, and layout of an Analog Phase-Locked Loop (APLL). The circuit consists of five major parts:

- A differential input, differential output Gilbert cell
- An off-chip RC low pass filter.
- A differential input, differential output voltage controlled oscillator (VCO)
- A differential to single-ended conversion for a single-ended output
- A startup circuit to allow the user to tune to approximately the desired frequency

The APLL is first given the signal to lock on to, called the reference signal, then a DC voltage is manually tuned to set the VCO to approximately the right frequency. When the frequency of the output is close to that of the input, the startup circuit will disconnect the user-supplied DC voltage and connect the output of the low-pass filter to the VCO. A pin is provided for a reset voltage. If the oscillator's tuning voltage goes below this voltage, the chip will be placed back into startup conditions. In simulation with parasitics, the APLL worked from approximately 4 MHz to 10 MHz. It operates with three voltage rails: -2.5 v, 0 v, and +2.5 v. Available outputs for monitoring are the differential tuning voltages of the VCO, the startup condition (logical high or low), the differential outputs of the VCO, and a single ended output from the difference of the two outputs.

Also included in the package is a separate VCO and Gilbert cell. There are four connections to each of these blocks. First the VCO has two input voltages and a differential output. Secondly, the Gilbert Cell has two inputs and a differential output.

The design and layout have been sent for fabrication through the MOSIS program. The characterization will be completed in the fall of 2007.

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I. Introduction

A. Project Objective

This report discusses the design and simulation of an Analog Phase-Locked Loop (APLL) in .5 μm CMOS Technology. The APLL takes an analog reference signal and produces an output operating at the same frequency with a phase shift from the reference dependent on that frequency. The objective of this project is summarized below:

1) Create an APLL with an off-chip low-pass filter
2) Design a method for which the APLL can operate over a range of frequencies
3) Fit the layout into a 900μm x 900μm area
4) Gain experience in circuit design and layout using Cadence®

It should be noted that a specific frequency range was not initially specified. With a complex circuit such as this APLL, the major goal was to make each of the components work together rather than spend time making them work at high frequencies. The APLL has been simulation from 4 MHz to 10 MHz.

There are five major parts to the circuit. Namely there is a Gilbert cell, an off-chip low-pass filter, a differential input, differential output voltage controlled oscillator (VCO), a manually controlled startup circuit, and a differential to single-ended conversion on the output. The design of each of these circuits will be discussed separately. Then the integration of the circuits will be discussed. The first thing to address is the theoretical workings of a phase-locked loop.

B. Overview of the Operation of an APLL

The basic flow of the APLL is shown in Figure 1. The first block is the Gilbert cell. It takes the input reference signal and multiplies it with the output signal. This is shown in Equation 1.

$$(A\sin(\alpha t+\phi_a))B\sin(\beta+\phi_b)) = \frac{AB}{2}(\cos((\alpha-\beta)t+\phi_a-\phi_b)+\cos((\alpha+\beta)t+\phi_a+\phi_b) \quad (1)$$

From this equation you can see that the arguments of the right side cosine functions are the frequencies of the two signals both subtracted and added creating what is known as the sum and difference frequencies. The goal is for α to equal β. When this is the case the difference cosine in Equation 1 is not dependent on time and therefore has a DC value proportional to the phase of the two signals. This DC value is what is needed to tune the output.

To analyze just the difference frequency value, a low-pass filter is used to remove the sum frequency from

Equation 1. This filtering is done off-chip with passive components. The low frequency signal is then used to drive the tuning voltage on the VCO. Eventually the output signal will be at the same frequency as the input signal and the low frequency signal will be a DC voltage relative to the phase difference between the two signals and the operating frequency. By using that signal to control the VCO, the output frequency will be constant with a phase relative to the frequency.

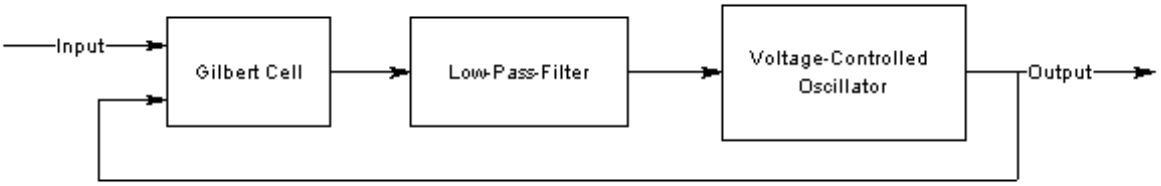


Fig. 1. Flow diagram of an APLL

II. Part II: Design, Simulation, and Layout

This section discusses the specifics of the circuits, the considerations to be taken for simulations, the other components on the chip, and the layout techniques.

A. Circuit Components

Each of the components in Figure 2 will now be analyzed. Though much of the design was first done without consideration to other components in the circuit, the later integration played a key role in the final design choices. It is important to note that the simulation results shown are simulations after parasitics have been extracted from the layout.

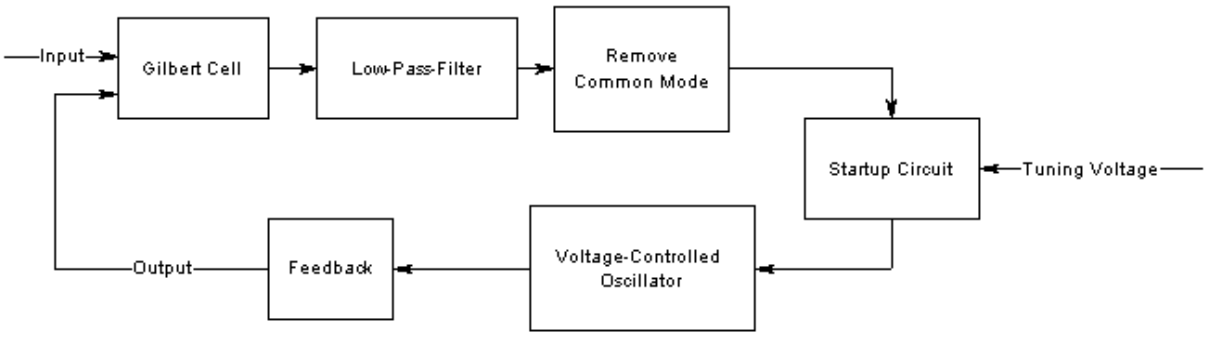


Fig. 2. Top level flow diagram of this APLL

1) Operational Amplifier: The operational amplifier (op-amp) is a crucial part to the operation of many modern analog circuits. There are op-amp's throughout the APLL. The circuit used for this project is shown in Figure 3. The op-amp has an NMOS input differential pair for the first stage. It uses a cascode

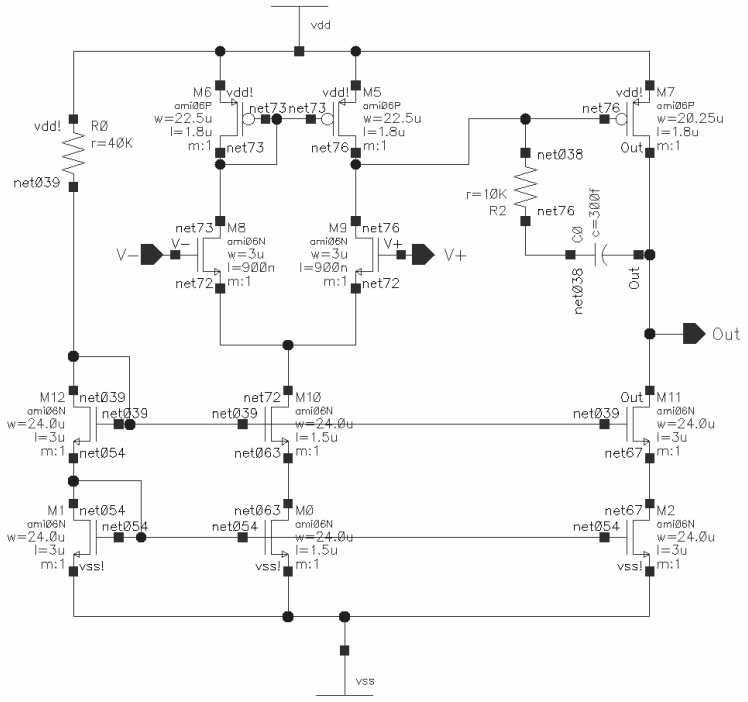
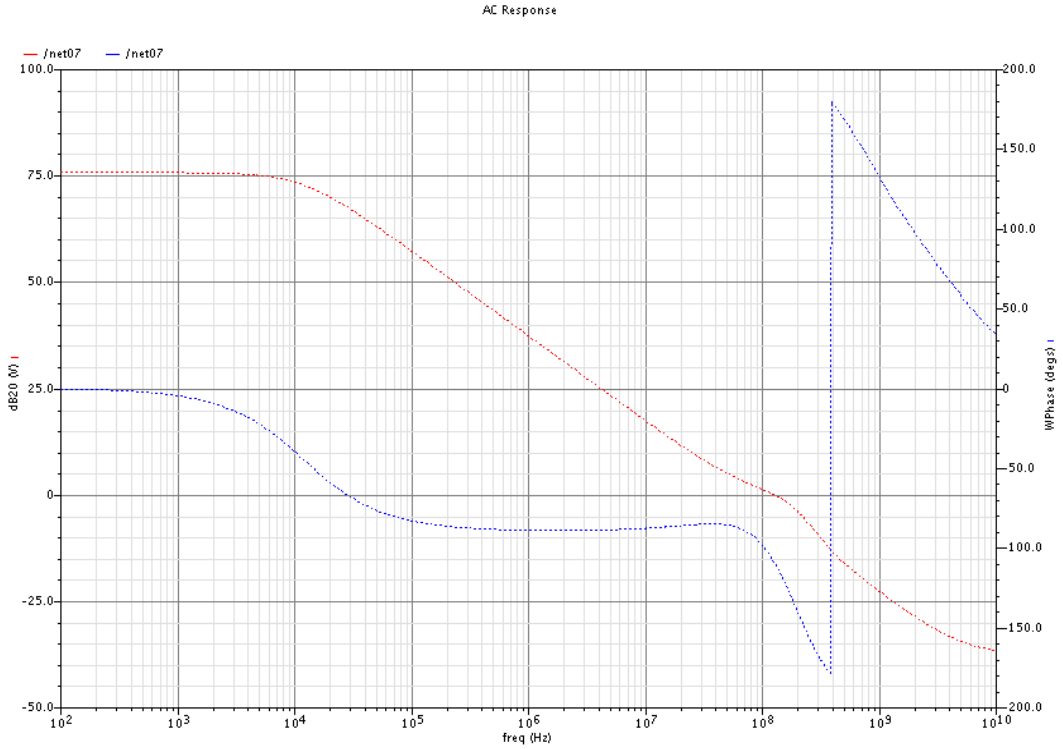
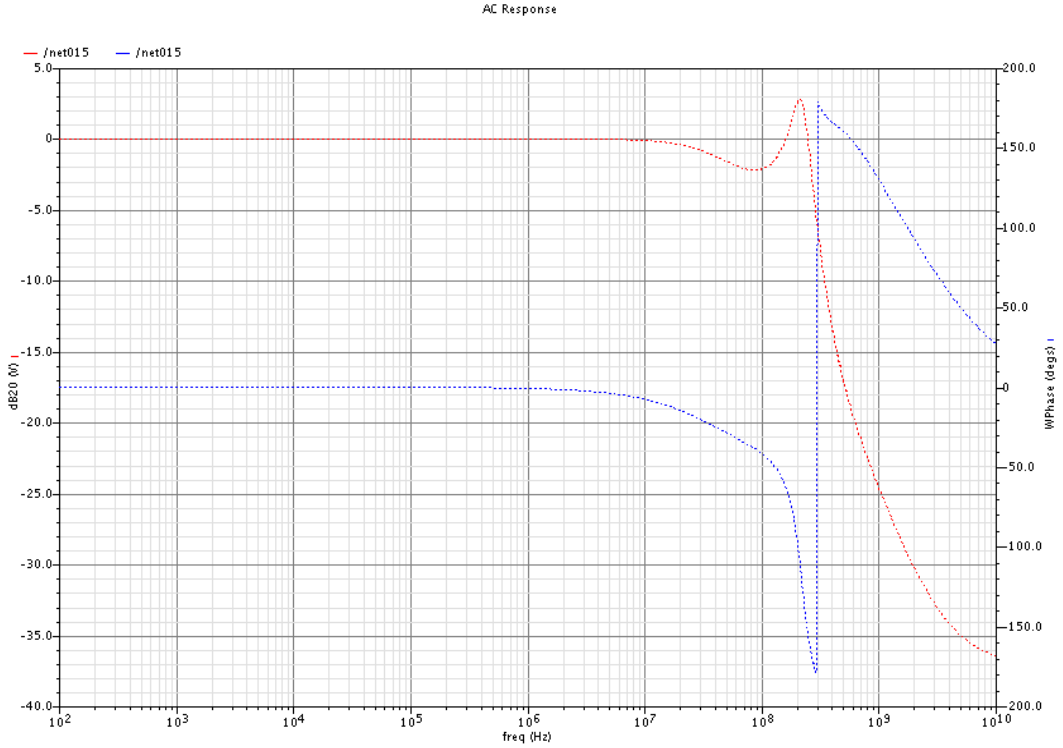


Fig. 3. Two-Stage Op-Amp

current source with a resistor to set the reference current. It uses an active PMOS load as the load. The second stage of the amplifier is a common source PMOS biased with the same cascode current source (with half sized transistors). A Miller capacitor and zeroing resistor are included for stability purposes. Without an output buffer the op-amp is not capable of driving large loads and therefore has a high output impedance. The open-loop frequency response of the op-amp is shown in Figure 4(a). The phase margin of the op-amp is 73^o. The unity gain frequency, f_t, is 125.7 MHz. The op-amp is typically used as a buffer in the circuit, so the unity feedback closed-loop response is of interest. This can be seen in Figure 4(b).



(a) Open-Loop response



(b) Closed-Loop response

Fig. 4. Op-amp frequency response

2) Single-Ended to Differential Conversion: The input of the APLL is a single-ended signal, but the Gilbert cell and APLL are differential input and output. Therefore a single-ended to differential conversion is done on-chip for both the DC tuning voltage to control the VCO on startup, and for the input reference signal. It is also used for removing common-mode signal from the differential output of the off-chip low-pass filter. A schematic of the single-ended to differential conversion is shown in Figure 5. One of the

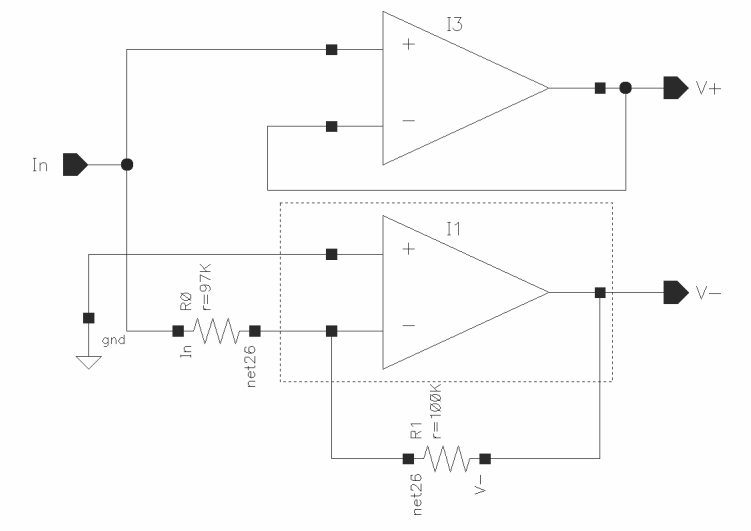


Fig. 5. Single-ended to differential conversion

op-amps is set up as a buffer and the signal is passed directly through the converter. The other op-amp is setup in an inverting configuration to create the inverse of the signal. As you can see the feedback of the inverting op-amp doesn't provide unity gain. This is because the op-amp's gain is low when driving resistive loads and the output was slightly smaller than when it was used as a buffer. The difference in values compensates for this.

3) Gilbert Cell: The Gilbert cell is where the multiplication of the two signals is performed. It is differential input and differential output. Figure 6 shows the schematic of the Gilbert cell. The theory behind the Gilbert cell is that the currents from each of the signals will sum through one of the resistors depending on the amplitude of the relative signals. The resistors as well as the bias current can be changed to influence the magnitude of the output. They also had to be adjusted to get the DC output close to zero volts. This proved to be an issue that was addressed by removing the common-mode signal later in the circuit.

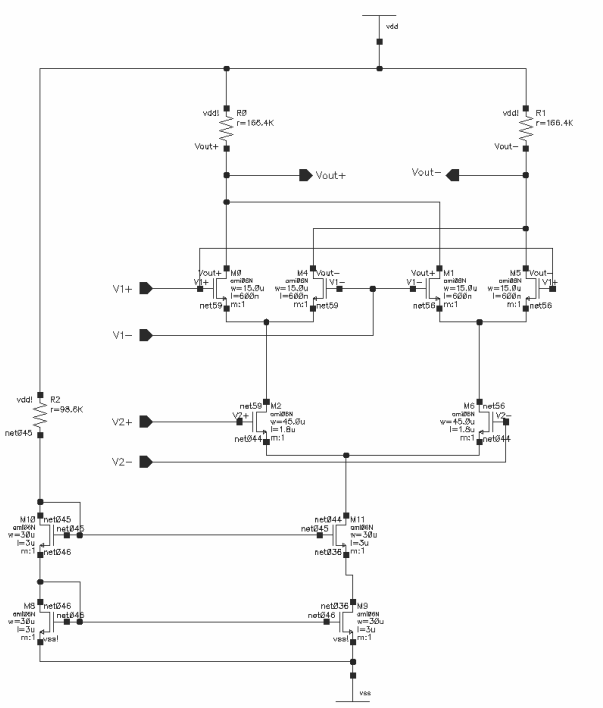


Fig. 6. Gilbert Cell schematic

4) Off-Chip Low-Pass Filter: The low-pass filter (LPF) is a simple RC filter. This is a portion of the circuit that can easily be changed by a tester in the lab. The best value could vary depending on the frequency that is desired. The schematic for the filter can be seen in Figure 7. As you can see this is a first order filter with a DC bleed-off capacitor for any charge that gets dumped onto the capacitor during the startup switch. It should be kept at a large value relative to the input resistor. The transfer function for this circuit can be seen in Equation 2.

$$T(s) = \frac{\frac{R_2}{R_1 C}}{s + \frac{R_1 + R_2}{R_1 R_2 C}} \tag{2}$$

The actual values to choose for the LPF components can vary based on the desired operating frequency range. Theoretically the pole should be set so that the sum frequency is attenuated and the difference frequency is preserved. It is most beneficial to move the pole to a lower value in order to take into consideration voltage amplitudes of the differential VCO. As frequency changes the amplitudes slightly change in the VCO. This amplitude change is not desired, but an effect of the design of the circuit. If the pole is to high, then the amplitude changes will oscillate and feed back through the LPF causing the

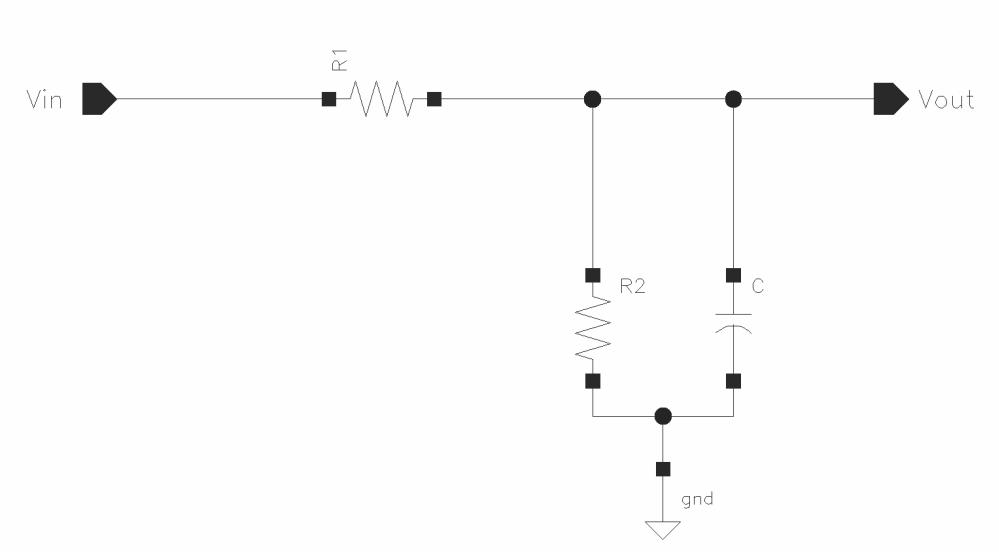


Fig. 7. Off-chip low-pass filter

frequency to be modulated. If this is seen in implementation it is recommended to slightly increase R_1 or C. Values for testing are discussed later in the report.

5) Removing Common-Mode Signal: Through simulation it was found that the signal from the LPF had a common-mode component. This is due to a common-mode output from the Gilbert cell. In order to remove this, the difference of the signals was taken, divided by two, and then put through a single-ended to differential conversion from Figure 5. The schematic for this portion is shown in Figure 8.

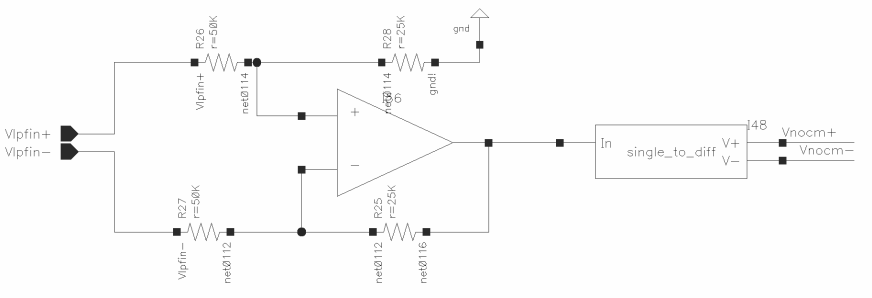


Fig. 8. Common-Mode removal

6) Startup Circuit: It was quickly discovered that a startup circuit was essential for the operation of this circuit. The purpose of the startup circuit is to allow the output frequency of the VCO to approach the desired frequency before the APLL tries to lock-on. This problem roots from the VCO not oscillating with a zero volt input. The top-level of the startup circuit is shown in Figure 9. The user inputs a DC

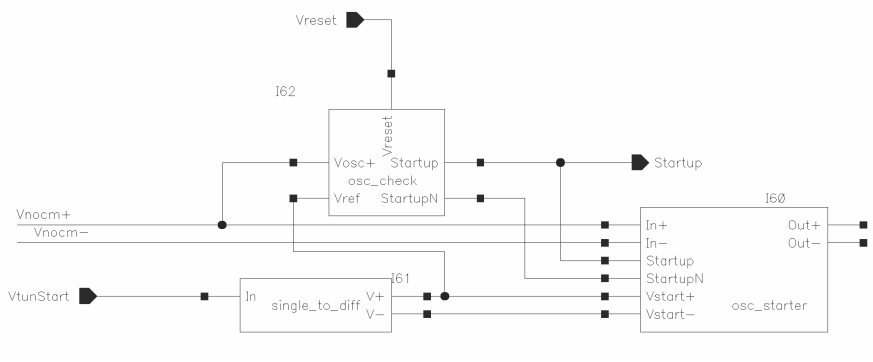
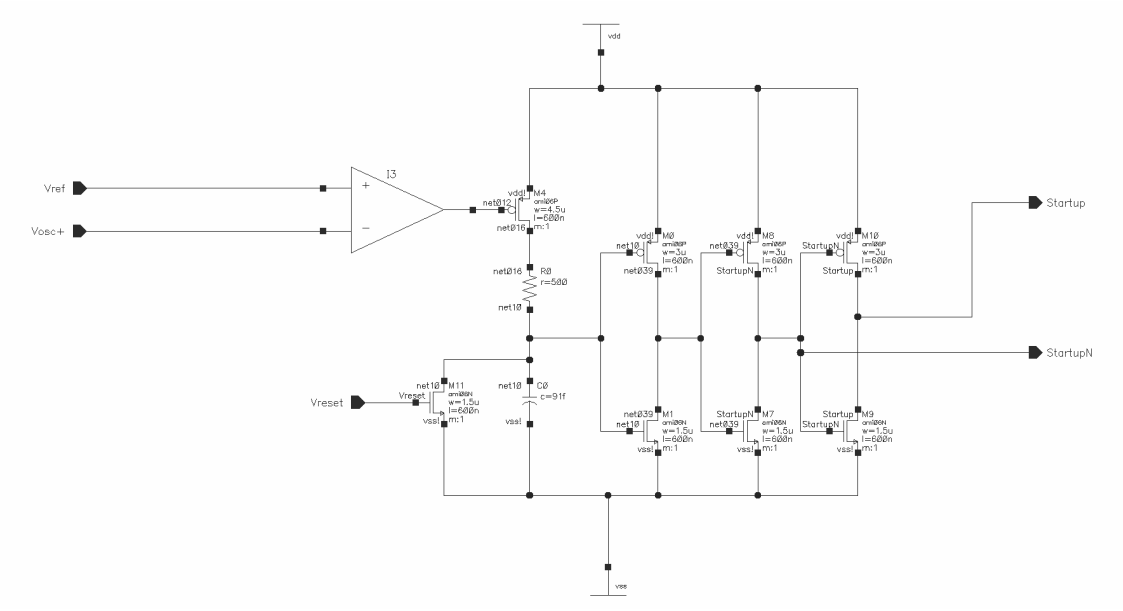
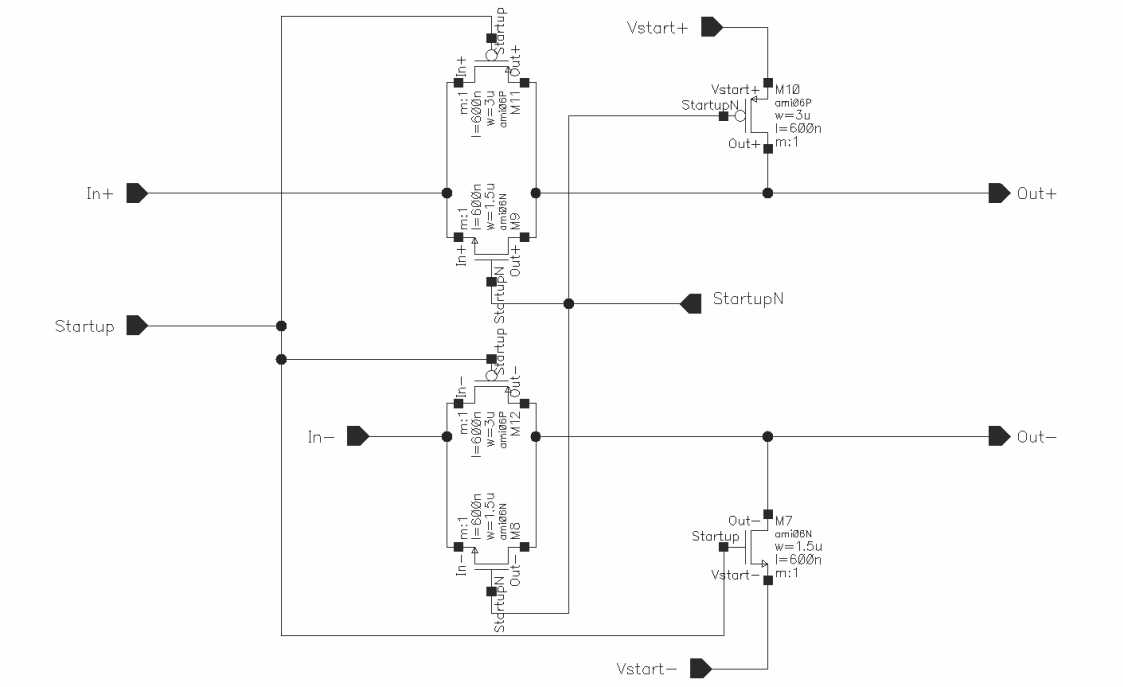


Fig. 9. Startup Circuit

voltage, this is converted into a differential voltage, and the startup circuit uses this voltage to run the oscillator. When the output of the LPF (with the common-mode removed) passes the magnitude of the tuning voltage, the startup circuit is removed and the APLL is allowed to lock-on to the frequency. Also included is a reset voltage control. This value is the minimum voltage that the output of the LPF (with the common-mode removed) can have. If it is crossed the APLL is returned to startup conditions. The oscillation check block (Figure 10(a)) checks if the LPF output is sufficient to operate the VCO and creates the startup signal. The startup signal is fed into the oscillation starter block (Figure 10(b)), which uses transmission gates and pass gates to decide which input should control the VCO.



(a) Checks to see if the APLL is ready to operate



(b) Sets the control of the VCO based on startup conditions

Fig. 10. Startup circuitry

7) Differential Voltage Controlled Oscillator: The VCO is composed of four Operational Transconductance Amplifiers (OTA's). The schematic for this design is shown in Figure 11. As you can see the input to the VCO is buffered through two op-amps. The first two OTA's provide the oscillation signal. The

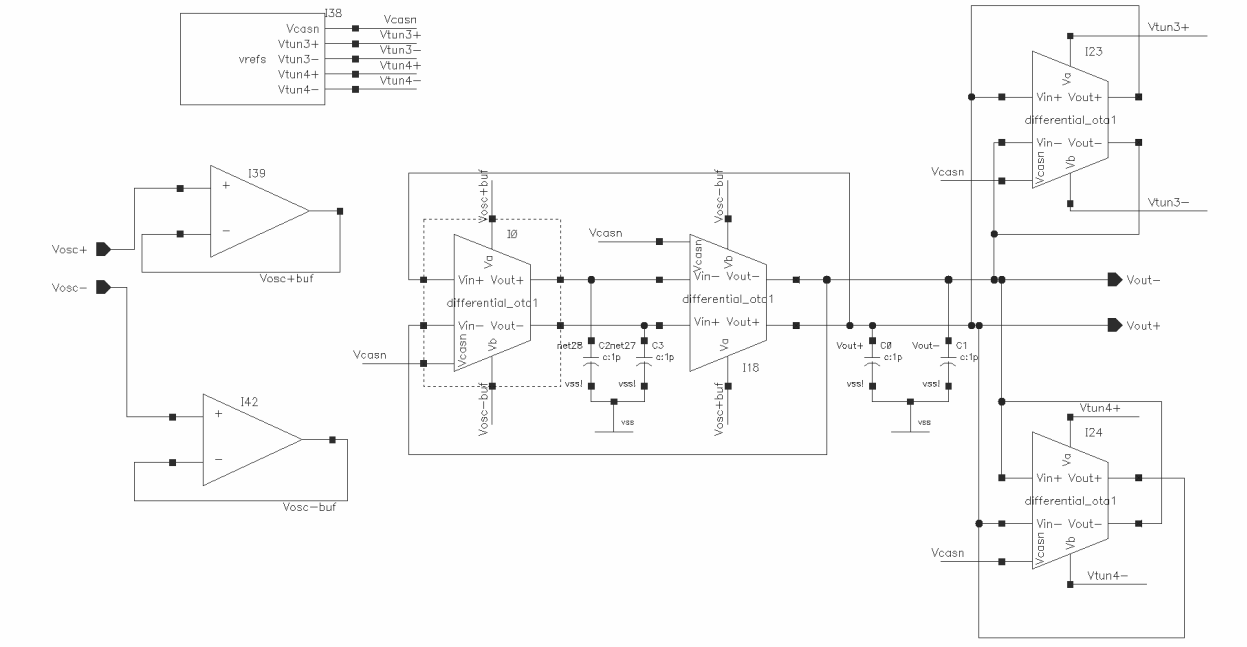


Fig. 11. Differential voltage controlled oscillator

third OTA (in the upper-right corner) provides reduced feedback at the peaks of the oscillating signal. The fourth OTA (in the lower-right corner) provides an ensured startup for the signal. By increasing the differential controls of the first two OTA's, the frequency is increased. By increasing the differential control of the third OTA, the amplitude of the signal is changed. The differential controls of the fourth OTA will effect both the frequency and magnitude of the oscillator, but it simply needs to have a value greater than zero in order to start the oscillator. The controls for the third and fourth OTA are set using resistive voltage dividers to a constant DC value. Also in the schematic are four capacitors. The capacitors are charged by the output of the OTA and provide a voltage on the inputs. The size of the capacitors will change the frequency of the oscillation as well. They were all chosen to be 1 pF. The schematic of the OTA is shown in Figure 12. The analysis of the VCO and OTA is completed in [1].

An in depth analysis of the VCO was done for frequency vs. tuning voltage. This can be seen in Figure 13. As you can see the frequency is not linear over voltage. Therefore some frequencies are harder to lock on to over others because there is a greater frequency shift for a small shift in tuning voltage.

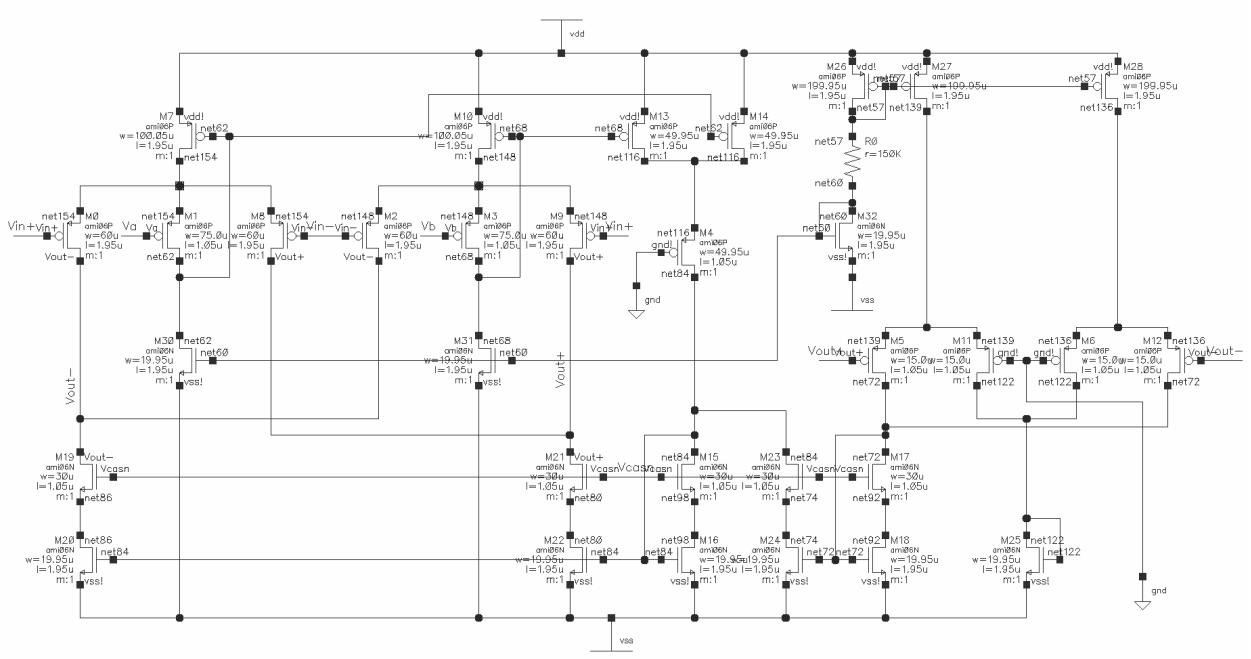


Fig. 12. Differential operational transconductance amplifier

8) Feedback and Output: The part that ties the APLL together is the feedback of the output to the Gilbert cell, allowing the APLL to lock-on to the desired frequency. The input to the Gilbert cell has to be small because it amplifies. To solve this an op-amp was used for attenuation. This was also beneficial because it provided a buffer to the output of the VCO. The schematic of the feedback path is shown in Figure 14. There are also two blocking capacitors shown. This allows the DC component of the feedback to be removed from the signal such as to not affect the DC biasing of the Gilbert cell. Also in this section is the difference amplifier used to get a single ended output. There is some amplification to the difference amplifier. This provides an output larger than the 50 mV signal going to the Gilbert cell.

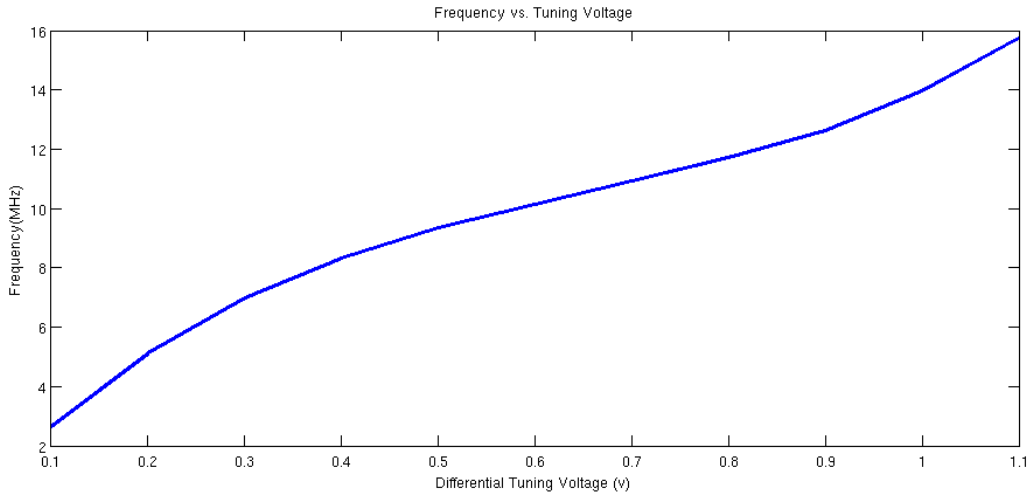


Fig. 13. Frequency vs. tuning voltage

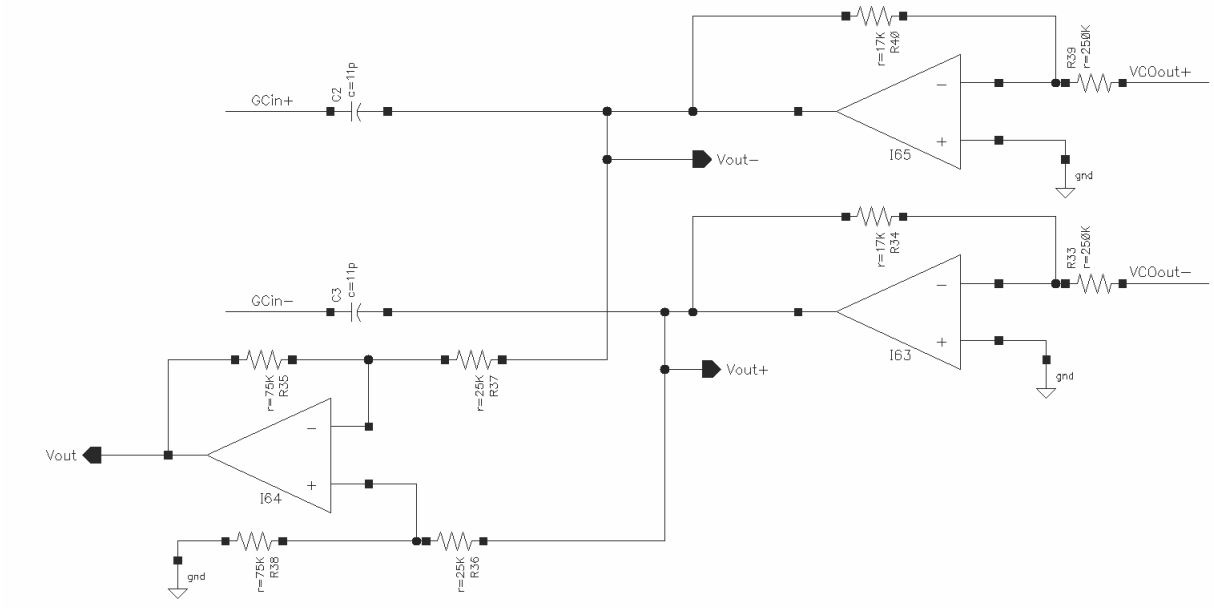


Fig. 14. Feedback of output and creation of single-ended output

B. Simulation Results

The simulation of the APLL presents some difficulties. The DC tuning voltage must be adjusted through the desired operation frequency so that the startup circuit will take over. Simulation conditions were discovered through trial and error. For this reason it is possible that through the proper scenario, the APLL could operate at higher and lower frequencies than those simulated. The outputs of interest are generally the tuning voltages of the oscillator, and the outputs of the low-pass-filter. They are easy to monitor, and easier to decipher compared to the VCO output. Therefore the simulations generally show these outputs rather than the VCO output.

C. Additional Devices on the Chip

Also included with the APLL is a separate differential VCO and a Gilbert cell. The inputs and outputs are buffered. The VCO has two pins for adjusting the differential tuning voltage. It also has a differential output (no single-ended conversion). The Gilbert cell has two single ended inputs. Through a single-ended to differential conversion they are buffered and then run through the Gilbert cell. The differential output is buffered before being directed off chip. These devices can be tested separately from the APLL. The testing is discussed in section III.

D. Pin-Out Table

TABLE I

PIN-OUT

Pin	Purpose	Pin	Purpose
1	NC	21	*Gnd*
2	Output of LPF -	22	Gilbert cell 2 Output +
3	Reference Input	23	Gilbert cell 2 Output -
4	Output of LPF +	24	NC
5	Reset Voltage	25	NC
6	NC	26	Gilbert cell 2 Input 1
7	NC	27	NC
8	NC	28	Gilbert cell 2 Input 2
9	Startup Output	29	Single-ended Output
10	Input to LPF -	30	Output +
11	Input to LPF +	31	Output -
12	NC	32	NC
13	NC	33	NC
14	NC	34	NC
15	NC	35	NC
16	VCO 2 Tuning -	36	NC
17	VCO 2 Tuning +	37	APLL VCO Tuning +
18	VCO 2 Output +	38	Input DC Startup Tuning Voltage
19	VCO 2 Output -	39	APLL VCO Tuning -
20	*Vss*	40	*Vdd*

E. Layout

The next portion of the project was the layout. Layout is always a key part of design. The major issue presented in this layout was that changes in capacitance on the nodes related to the oscillator can affect the frequency of the oscillator relative to the differential tuning voltage. This is not really a problem, but only a hassle when it comes to simulation. The simulation conditions that were found for simulating the schematic no longer fit with the layout and new conditions had to be found.

The layout was done using two layers of metal except for on the top level to access *Vdd*, *Vss*, and *Gnd*. Also, specific care was taken to ensure that there were no contact connections made through a single via contact. The reason for this is to prevent the case where one of the contacts doesn't open up. A second contact protects against this.

Another point to notice is that there is a low-frequency portion of the circuit consisting of the startup circuit and common-mode removal circuit. To prevent noise from the high frequency output of the Gilbert cell, the low frequency portion was placed in a protective ring. This can be seen in Figure 15. There is a ring of metals 3, 2, and 1 with poly under the ring. The poly and metal 1 are connected together and are also connected to *Vss*. Metal 2 is connected to *Gnd*, and metal 3 is connected to *Vdd*. For connections in and out of the block a break is made in metal 1. Hopefully this will prevent noise from entering the ring from the other portions of the circuit.

The final layout was placed in the bonding pad ring. The design was eventually simulated at the top level. Again, the added capacitance slightly affected the oscillation frequency of the VCO changing the simulation conditions. A simulation of the top level is shown in Figures 16, **??**, and **??**. This shows the tuning voltages locking onto the proper DC value. It is also important to note that the layout passed both DRC and LVS at the top level before and after stream out. A copy of the LVS results is included in the appendix.

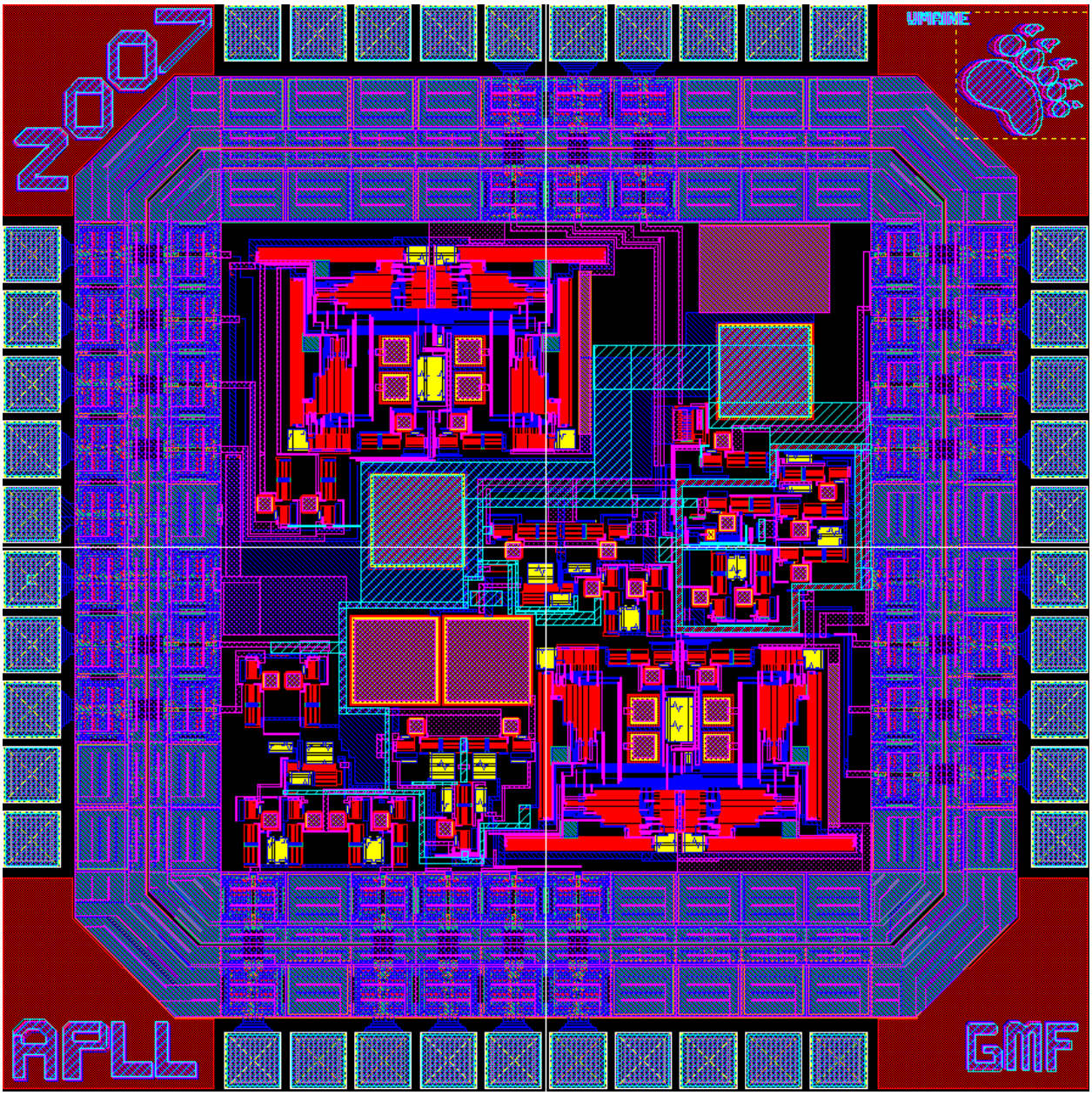


Fig. 15. Layout of APLL

III. Test Procedures and Protocols

This section discusses some testing procedures for characterizing this chip. First of all tests for the normal characteristics of the APLL are included for a range of frequencies. Also a test for power consumption is included. Then the seperate Gilbert cell and VCO are addressed and testing procedures are included.

A. APLL Lock-on Test 1: 4 MHz

This section discusses the lock-on of the APLL at 4 MHz. First the circuits for the low-pass filter will need to be made. Table II has the component values corresponding to the individual components of the LPF. The components correspond to Figure 7 on page 11. The following equipment is necessary for the

TABLE II

Low-Pass Filter Component Values: 4 MHz

Component	Value
R_1	250 kΩ
R_2	10 MΩ
C	300 pF

testing:

- DC voltage supply providing ± 2.5 volts
- Tunable DC voltage supply providing 50 mV to 500 mV
- DC voltage of 25 mV from a separate voltage supply -or- from a resistor divider network using the ± 2.5 volt supply
- Signal generator capable of creating a 50 mV peak 4 MHz sin wave
- Oscilloscope with multiple input channels (at least 4) or multiple oscilloscopes

The following steps outline the assembly and testing of the APLL at 4 MHz. *Do not turn on any of the voltage supplies until told to do so!*

1) Construct the low-pass filter from the values in Table II. Remember that two filters must be constructed, one for each end of the differential signal.
2) Connect the inputs of the low-pass filter to pins 10 and 11
3) Connect the outputs of the low-pass filter to pins 2 and 4
4) Connect the ± 2.5 volt power supply to *Vdd* (pin 40), *Vss* (pin 20), and *Gnd* (pin 21).

5) Connect the tunable DC voltage supply for starting the APLL to pin 38 (and the *Gnd* node to pin 21)
6) Connect the reset voltage to pin 5. It is recommended that this be connected to 25 mV. The 25 mV can either be from a separate supply, or a voltage divider of 100k and 900k can be used between *Vdd* and *Gnd*. (Or any other combination of resistors that achieves this value).
7) In order to ensure that the other devices on the chip are not operating, connect pins 16-19, 22, 23, 26, and 27 to *Gnd*.
8) Connect the reference from a signal generator to pin 3
9) Monitor the following with an oscilloscope:
    - Input Reference (pin 3)
    - Output Signal (pin 29)
    - The tuning voltage on the VCO on pins 37 and 39
    - The startup condition (pin 9)
10) Turn all the power supplies on. Set the tuning voltage (pin 38) to 200 mV
11) Turn on the the reference input signal and set the amplitude to 50 mV amplitude and 4 MHz frequency
12) Monitor the output of the APLL and decrease the tuning voltage (pin 38) until it approaches the appropriate frequency. The startup signal (pin 9) should go low. At this point the APLL is attempting to lock-on to the reference.
13) Monitor the differential tuning voltages of the VCO. They should eventually approach a DC value that corresponds to 4 MHz. A simulation of the output of the LPF as it approaches then locks to the tuning voltage is shown in Figure 16.
14) If the APLL is not locking on (the startup pin doesn't stay low), the recommended solution is to increase the capacitor in the low-pass filter and repeat this procedure

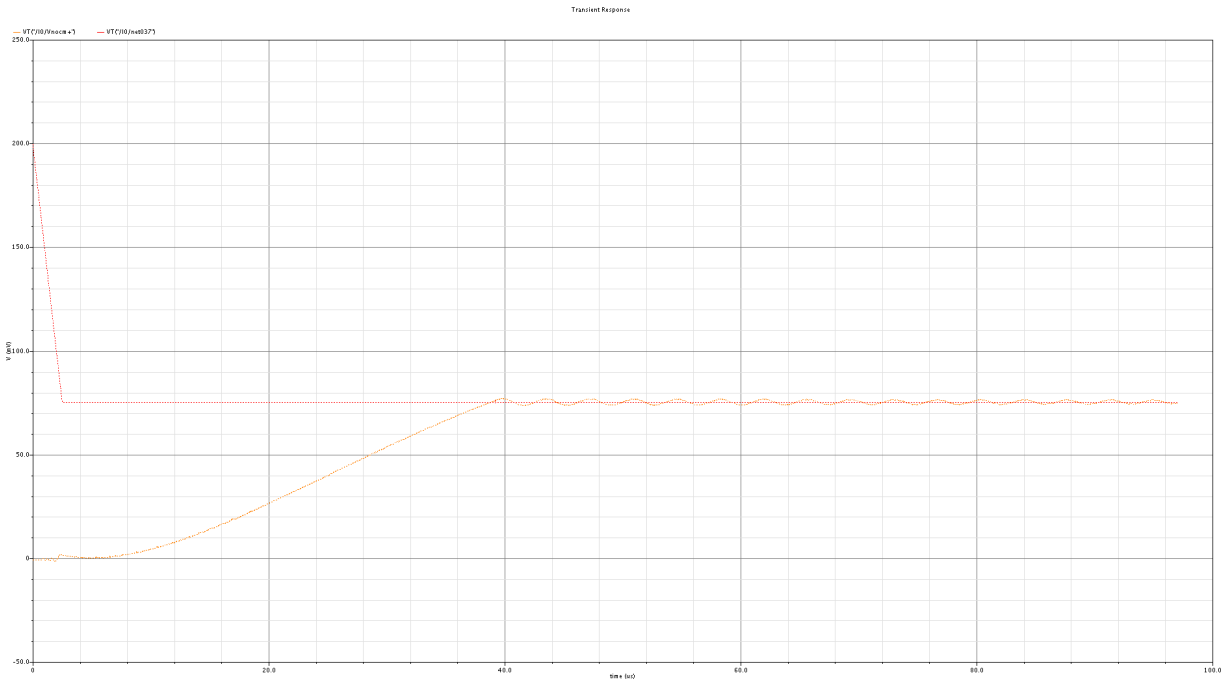


Fig. 16. Simulation with parasitics of APLL lock-on to 4 MHz

B. APLL Lock-on Test 2: 7 MHz

This section discusses the lock-on of the APLL at 7 MHz. First the circuits for the low-pass filter will need to be made. Table III has the component values corresponding to the individual components of the LPF. The components correspond to Figure 7 on page 11 To test this frequency follow the steps

TABLE III

LOW-PASS FILTER COMPONENT VALUES: 7 MHZ

Component	Value
R_1	100 kΩ
R_2	10 MΩ
C	200 pF

in section III-A with the following differences:

- In step 1 build the low-pass filter in Table III.
- In step 10 initially start the tuning voltage at 400 mV

The results of this are similar to Figure 16. The difference is that the tuning voltage should be around 150 mV when the APLL locks-on.

C. APLL Lock-on Test 3: 10 MHz

This section discusses the lock-on of the APLL at 10 MHz. First the circuits for the low-pass filter will need to be made. Table IV has the component values corresponding to the individual components of the LPF. The components correspond to Figure 7 on page 11 To test this frequency follow the steps

TABLE IV

LOW-PASS FILTER COMPONENT VALUES: 10 MHZ

Component	Value
R_1	200 kΩ
R_2	10 MΩ
C	25 pF

in section III-A with the following differences:

- In step 1 build the low-pass filter in Table IV.
- In step 10 initially start the tuning voltage at 500 mV

The results of this are similar to Figure 16. The difference is that the tuning voltage should be around 300 mV when the APLL locks-on. Included in Figure 17 is a plot of the input and output after lock-on.

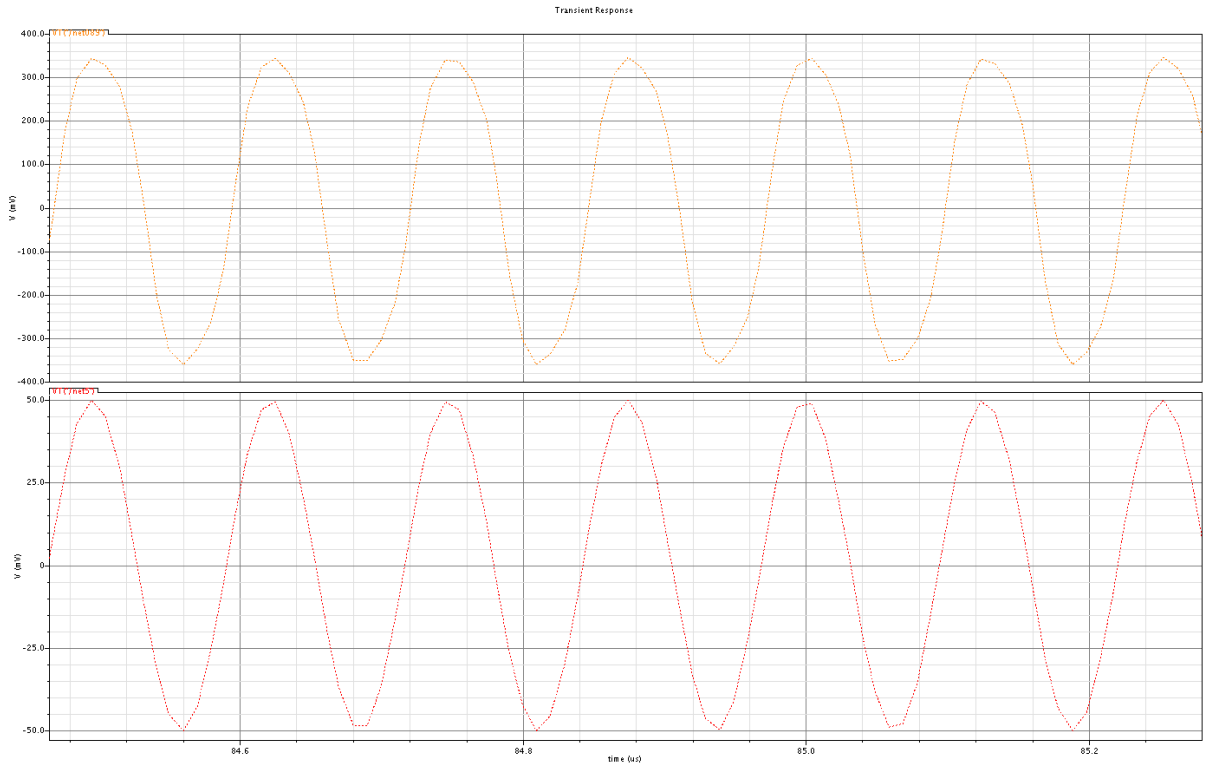


Fig. 17. Simulation with parasitics of APLL input and output after lock-on to 10 MHz

D. Power Consumption

This section will measure the average power consumption of the APLL by itself. The chip will be set up the same as in section III-A. The low-pass filter should be constructed using the values from Table II. Follow the steps to starting the APLL through step 10. The *Gnd* terminal is simply connected to capacitive nodes, therefore by measuring the current into *Vdd*, and then multiplying by 5 volts, the total power for the chip can be calculated. In simulation this value was 57 mW.

E. Separate Gilbert Cell Test With Low-Pass Filter

There is a separate Gilbert cell available for testing on the chip. In order to complete the testing of this device the following equipment is needed.

- DC voltage supply providing $\pm$ 2.5 volts
- Two signal generators with synchronized outputs
- An oscilloscope with an A-B difference capability
- The low-pass filter from Table II

The following steps outline how to perform this test on the Gilbert cell. The output of the low-pass filter will be the difference frequency between the input signals to the Gilbert cell. The following steps outline how to perform this test.

1) Connect *Vdd*, *Vss*, and *Gnd* to their respective pins.
2) To disable the APLL and second VCO connect the following pins to *Gnd*: 3 10 11 16 17 18 19 37 38 39.
3) Connect one of the signal generators to the Gilbert cell input 1 on pin 26. Connect the other signal generator to the Gilbert cell input 2 on pin 28
4) Connect the input of the low-pass filter to the outputs of the Gilbert cell on pins 22 and 23.
5) Monitor the difference of the two outputs of the low-pass filter.
6) Turn the power on to the chip
7) Set the signal generators to 50 mV peak amplitude with an output frequency of 4 MHz
8) Increment the frequency of the oscilloscope on pin 28 to 4.01 MHz. The output of the low-pass filter should be the difference frequency, or 10 kHz. This is shown in Figure 19.
9) As a second test again set the signals to both 4 MHz, then increase the phase of one of the signals by 45^o. The output should now be a differential DC value of approximately 500 mV.

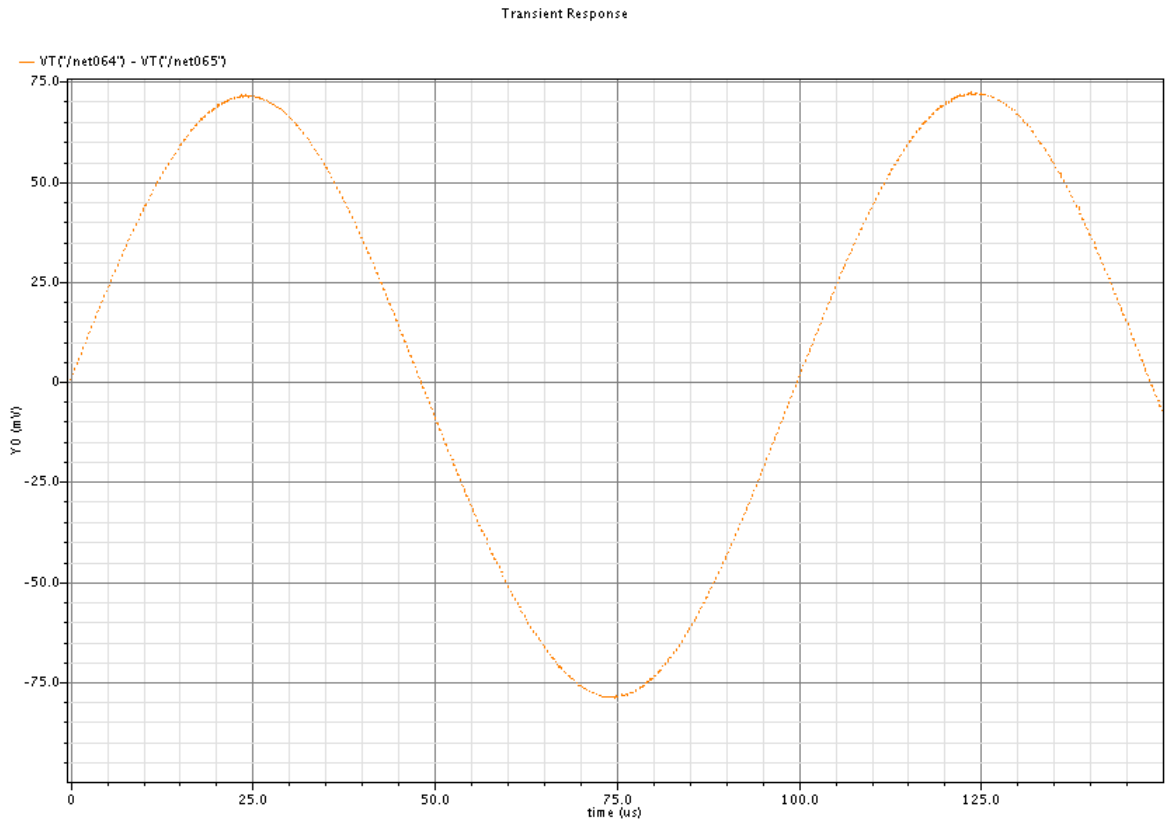


Fig. 18. The output of the Gilbert cell with inputs of 4 MHz and 4.01 MHz

F. Separate VCO test

There is a separate VCO available for testing on the chip. In order to perform this test the following equipment is needed:

- DC voltage supply providing $\pm$ 2.5 volts
- A DC power supply with differential output
- An oscilloscope with an A-B difference capability

This describes the testing of the VCO over a range of frequencies. It is important to note that the parasitic capacitance on each of the nodes of the VCO is different than the VCO in the APLL, so it's operating frequencies will be slightly different. The steps to performing this test are as follows:

1) Connect *Vdd*, *Vss*, and *Gnd* to their respective pins.
2) To disable the APLL and the Gilbert cell attach the following pins to *Gnd*: 3 10 11 22 23 26 28 37 38 39.
3) Connect the differential tuning voltage to pins 16 and 17.
4) Monitor the difference between pins 18 and 19.
5) Power up the chip and set the tuning voltage to $\pm$ 500 mV.
6) Set the tuning voltage to the values in Table V and compare the output frequency to the results of the simulation.

TABLE V

VCO SIMULATION TEST RESULTS

Tuning Voltage	Output Frequency (MHz)
$\pm$500 mV	14.3
$\pm$450 mV	13.0
$\pm$400 mV	11.9
$\pm$350 mV	11.1
$\pm$300 mV	10.3
$\pm$250 mV	9.43
$\pm$200 mV	8.38
$\pm$150 mV	7.04
$\pm$100 mV	5.09
$\pm$50 mV	2.64

IV. Conclusion

The design of an Analog Phase-Locked Loop has been completed through the stages of design, simulation, and layout. The APLL has been simulated as operational at 4, 7, and 10 MHz. With the capability of operation at different frequencies in this range. The APLL has a controllable startup scheme with reset on errors in the output based on a controllable reset voltage. The layout was completed passing both DRC and LVS at the top level. The design has been sent for fabrication and testing will proceed as described in this report upon the return of the fabricated devices in the fall of 2007.

A. Suggestions for Future Work

There are many different things that could be done to this APLL. Some suggestions are as follows:

- Most errors are caused by the non-linearity in amplitude, frequency, and distortion of the output of the VCO. It would be beneficial to address each of these problems in order to achieve a better output signal, with a more predictable response.
- The frequency of operation could be addressed by looking at things such as the VCO and the op-amp used in this circuit. They would both have to be improved to achieve this goal.
- A better startup scenario could be implemented with a possible control from a microprocessor to start the circuit. This would reduce the need of human control to start the APLL
- Automated gain control gain could be used on the input to allow for a range of magnitudes

Overall this was a successful project. the original task seemed daunting, but the final result was a succesful design, at least in simulation.

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Greg is from Holden, Maine and has been attending the University of Maine since September of 2003. He graduated from the undergraduate program in May of 2007. During his time at the university he was a member of Eta Kappa Nu and Tau Beta Pi. Currently he resides in Bedford, New Hampshire working for BAE systems doing IC design.

REFERENCES

[1] J. Galan, R. G. Carvajal, A. Torralba, F. Munoz, and J. Ramirez-Angulo, "A low-power low-voltage ota-c sinusoidal oscillator with a large tuning range," *IEEE Transactions on Circuits and Systems*, 2005.

APPENDIX

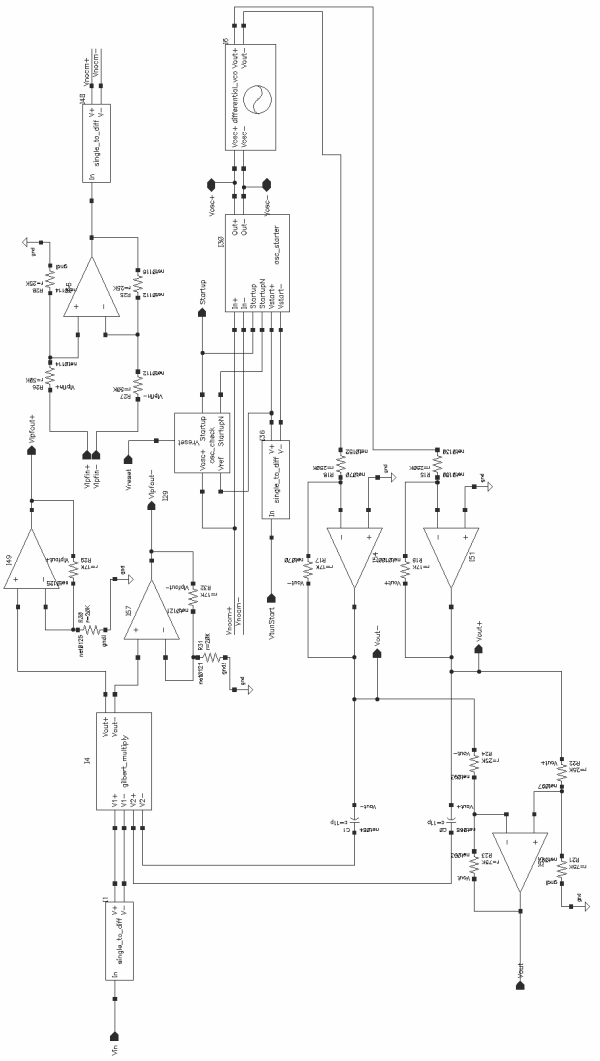

Fig. 19. Top level schematic of APLL