

Digital to Analog Converter

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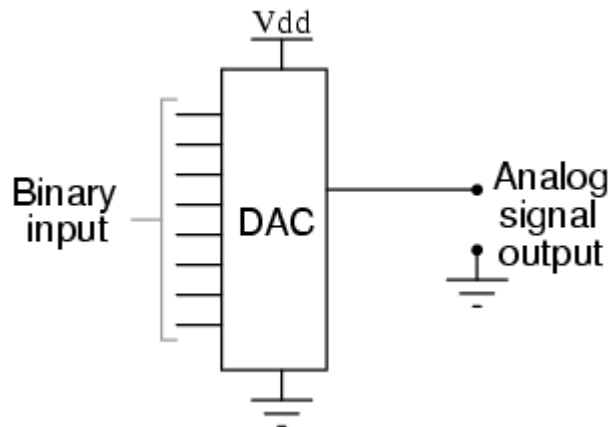
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1) INTRODUCTION

A **digital-to-analog converter (DAC or D-to-A)** is a device for converting a digital (usually binary) code to an analog signal (current, voltage or charges). Digital-to-Analog Converters are the interface between the abstract digital world and the analog real life. Simple switches, a network of resistors, current sources or capacitors may implement this conversion.

A DAC inputs a binary number and outputs an analog voltage or current signal. In block diagram form, it looks like this:



2) DAC types

The most common types of electronic DAC's are:

- The Pulse Width Modulator the simplest DAC type. A stable current (electricity) or voltage is switched into a low pass analog filter with a duration determined by the digital input code. This technique is often used for electric motor speed control, and is now becoming common in high-fidelity audio.
- **Oversampling DACs** such as the **Delta-Sigma DAC**, a pulse density conversion technique. The oversampling technique allows for the use of a lower resolution DAC internally. A simple 1-bit DAC is often chosen, as it is inherently linear. The DAC is driven with a pulse density modulated signal, created through negative feedback. The negative feedback will act as a high-pass filter for the quantization (signal processing) noise, thus pushing this noise out of the pass-band. Most very high resolution DACs (greater than 16 bits) are of this type due to its high linearity and low cost. Speeds of greater than 100 thousand samples per second and resolutions of 24 bits are attainable with Delta-Sigma DACs. Simple first order Delta-Sigma modulators or higher order topologies such as **MASH - 'Multi stage' noise Shaping** can be used to generate the pulse density signal. Higher oversampling rates relax the specifications of the output Low-pass filter and enable further suppression of quantization noise.
- The **Binary Weighted DAC**, which contains one resistor or current source for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision resistors and current-sources are expensive, so this type of converter is usually limited to 8-bit resolution or less.
- The **R2R Ladder DAC**, which is a binary weighted DAC that creates each value with a repeating structure of 2 resistor values, R and R times two. This improves DAC precision due to the ease of producing many equal matched values of resistors or current sources, but lowers conversion speed due to parasitic capacitance.
- The **Segmented DAC**, which contains an equal resistor or current source segment for each possible value of DAC output. An 8-bit binary-segmented DAC would have 255 segments, and a 16-bit binary-segmented DAC would have 65,535 segments. This is perhaps the fastest and highest precision DAC architecture but at the expense of high cost. Conversion speeds of >1 billion samples per second have been reached with this type of DAC.
- **Hybrid DACs**, which use a combination of the above techniques in a single converter. Most DAC integrated circuits are of this type due to the difficulty of getting low cost, high speed and high precision in one device.

3) DAC Presented

This paper will present the 12 bit binary weighted DAC.

The DAC operates at a maximum frequency of 25MHz using .6um technology to drive a load of 20pF.

3.1) Blocks of the DACs

The DAC consists of the following blocks

- 1) Binary weighted ladder.
- 2) Op-amp

3.2) Binary Weighted Ladder

The binary weighted ladder consists of 30K and 15K resistors placed in a configuration as shown in fig. The inputs to the ladder are fed from a 12 bit ROM. The input voltages range from 0V to 5V.

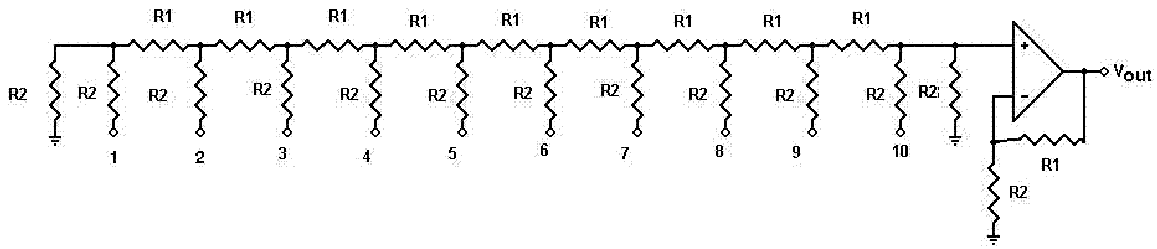
The output of the ladder is fed to an OP-AMP. It only supplies a voltage from 3.1V to 4.1 V as an output. Biasing for such an output range was decided by the characteristics of the OP-AMP.

Biasing was implemented using a buffer placed with the ladder network as shown in figure to maintain linearity in the DAC output.

So when all inputs are low, the ladder supplied a voltage of 3.1 V to the OP-AMP and when all the inputs are high a voltage of 4.1V was supplied.

For a 10 bit ladder and 0-5V rails

The accuracy needed is $5/1025 = 0.0049V$,



But this is the max voltage variation in both direction of the ideal voltage. Hence the variation from ideal output is $0.0049/2 = 0.00245V$

Which means that for every bit from the input, an analog voltage of 0.0049 is produced at the output.

From the ladder schematic the most stringent accuracy is needed when the input varies from 0111111111 to 1000000000

For such a transition $V_{out} = V_{ref} R1/R2 = 2.497V$

$R1/R2 = .1\%$

Which is the matching needed in this technology for linearity to be maintained in the output. .

Below is shown the schematic of the ladder in two stages.

- 1) One with the binary weighted resistors
- 2) One with the buffer placed for biasing the op-amp.

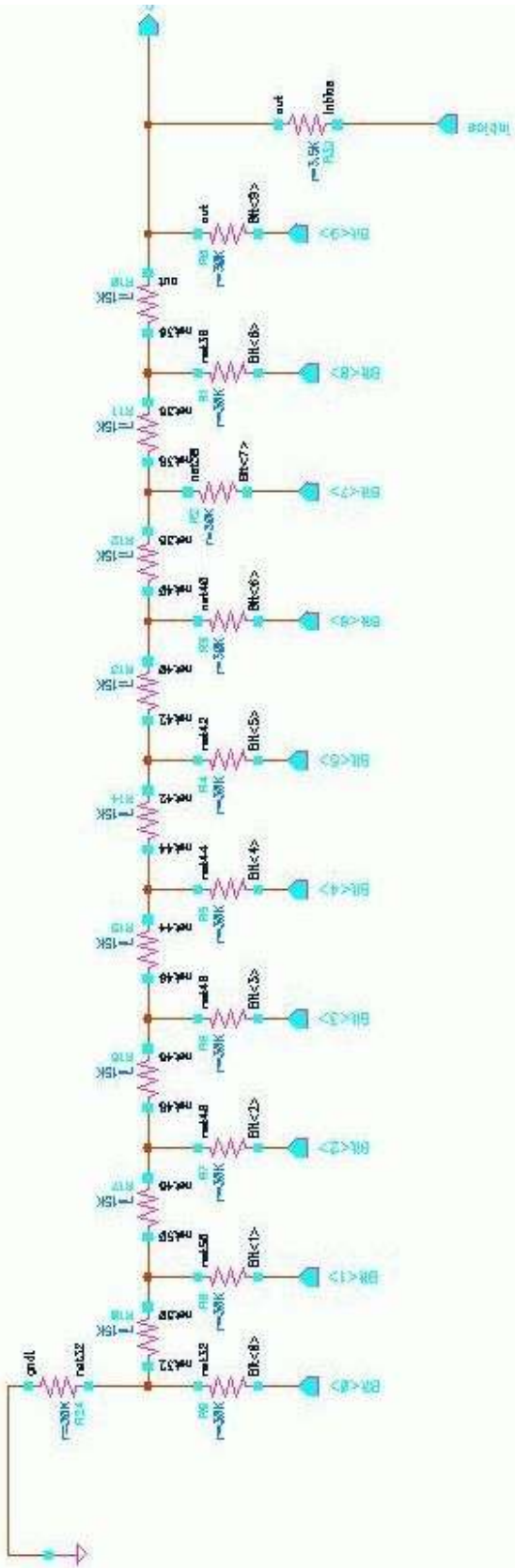
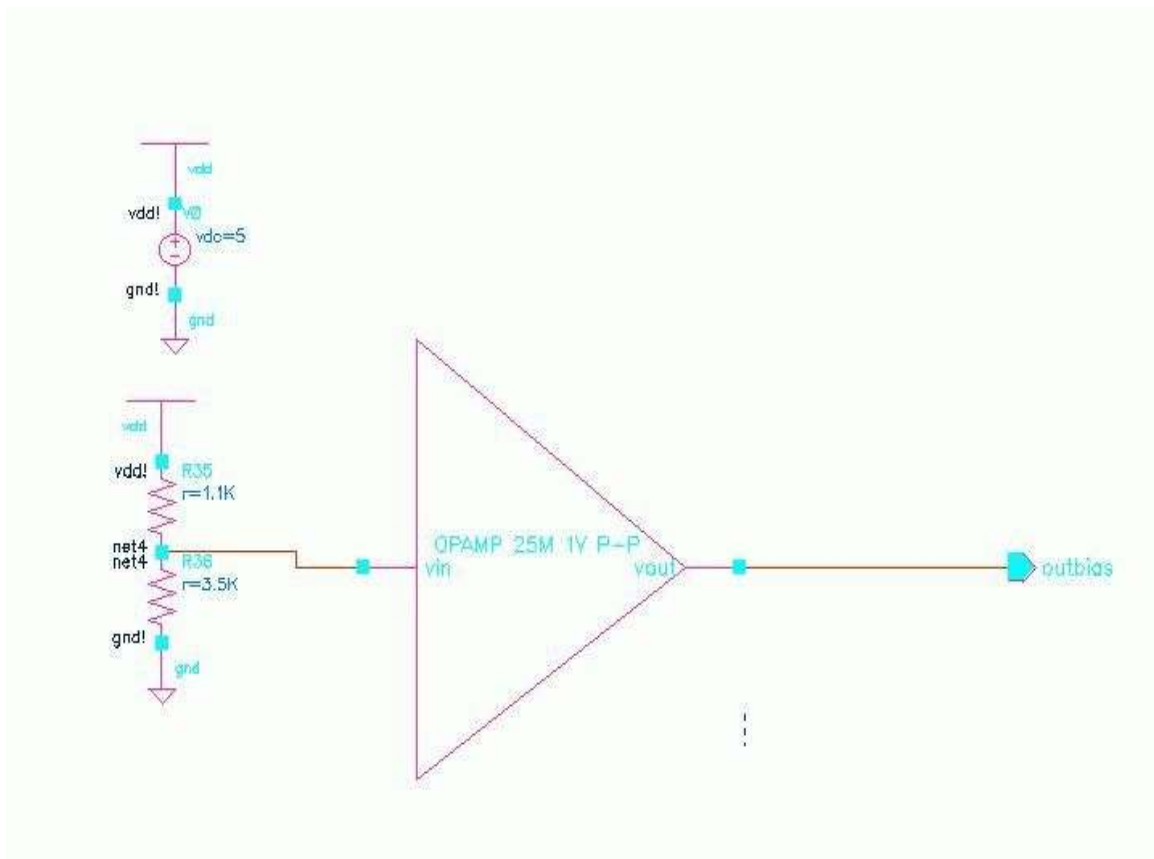
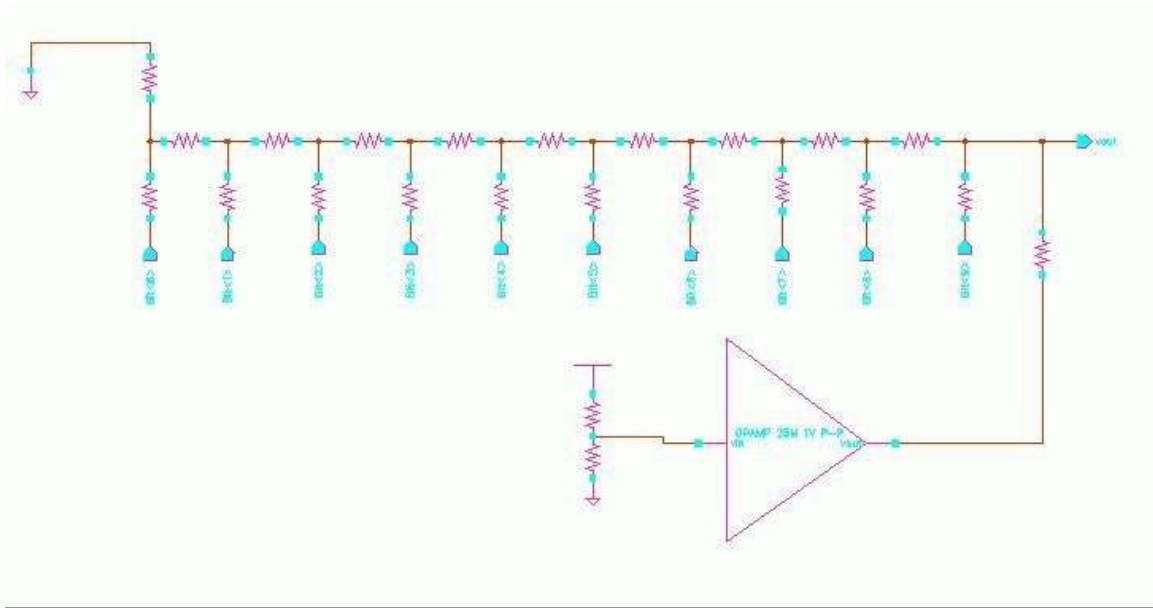


Figure of buffer for bias to op-amp



The complete schematic of the ladder including the biasing for the op-amp



3.3) OP-AMP

The design of the op-amp was based on the following design parameters-

- 1) 10 input bits
- 2) 0-5V rail voltages
- 3) 50Mhz clock frequency or 25Mhz frequency for DAC

3.4) OPEN LOOP GAIN

The op-amp in this DAC is used in unity feedback configuration.

The closed loop gain for an op-amp is given by $A/(A+1)$, where A is the open loop gain

The error V_{out}/V_{in} is highest at the highest possible V which is $V_{ref}=5V$

Hence A was calculated to be a minimum 2082.

3.5) GAIN BANDWIDTH

For a maximum operating frequency of 25Mhz, the output needs to be settled in 40ns
Again as in the calculation of the open-loop gain, the maximum speed is needed when the output voltage is the highest i.e. 5V

$$4.9976=5(1-e^{-(t/RC)})$$

$$RC=5.2ns$$

Or the gain bandwidth comes out to be 20Mhz

4) CIRCUIT DESIGN

The op-amp was designed to work in 2 stages

- 1) A differential first stage which works as an input for the binary ladder
- 2) Final gain stage for an output load of 20pF

4.1) BIASING CIRCUIT

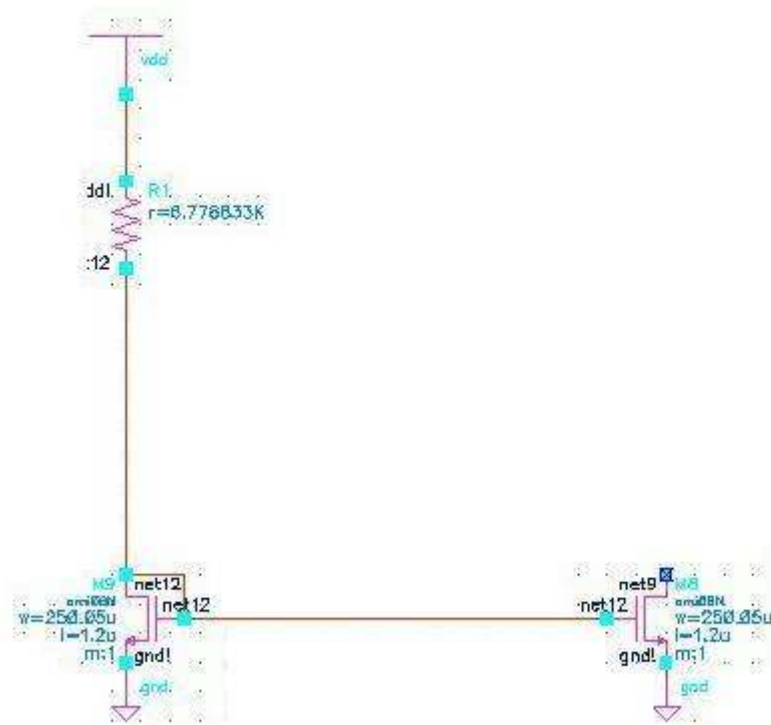
The biasing circuit for the op-amp was implemented using p-mos current mirrors and n-mos current sources for both the stages.

To avoid the affect of slew rate on the op-amp the current to be delivered in the first stage was calculated to be 600uA

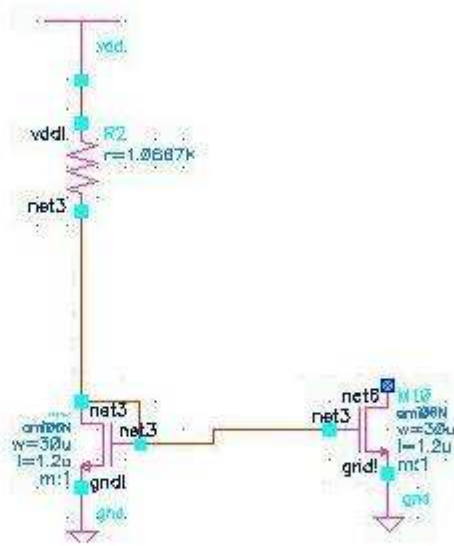
The current in the 2nd stage was calculated from the 1st stage to be about 2.3mA.

Schematics of the biasing stages are shown in fig

Bias circuit schematic of 1st stage of op-amp



Bias circuit schematic of 2nd stage of op-amp

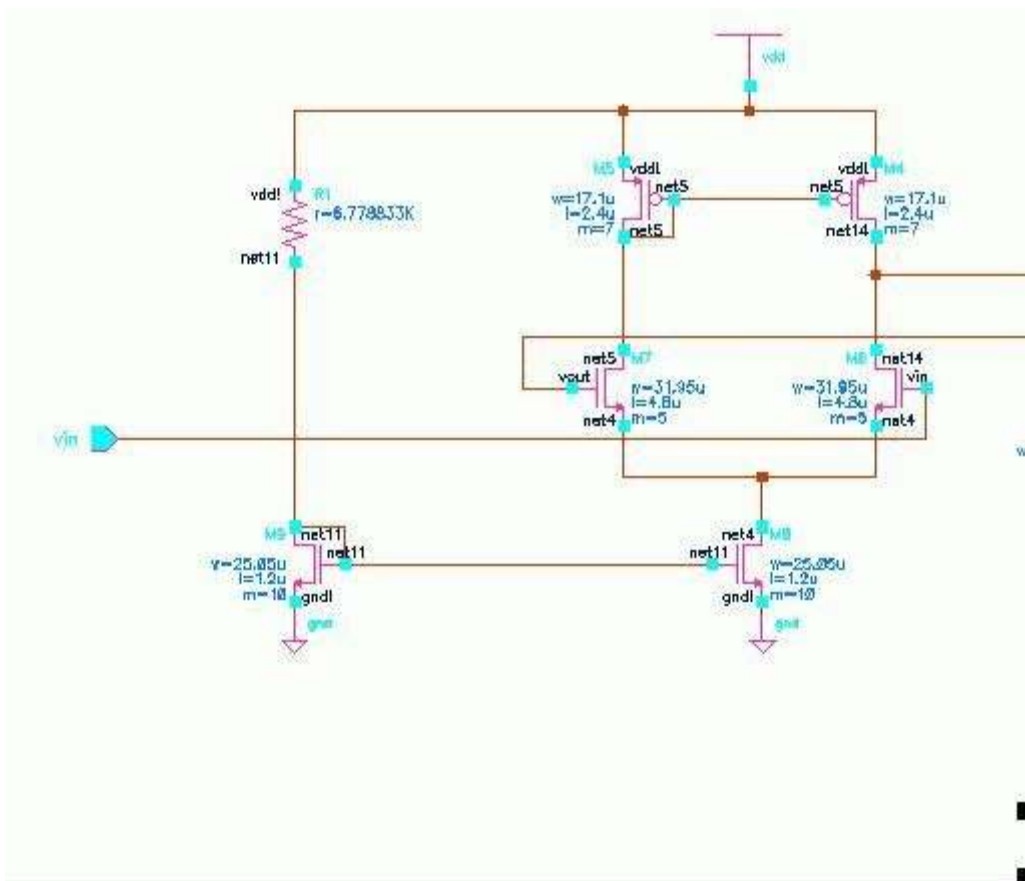


4.2) FIRST STAGE

The first stage of the op-amp as shown in the fig gives a gain of about 45-60 from a common mode range of 3-4V.

Sizes of the transistors are given in fig.

The lengths of transistors had to be increased to provide high small signal output impedance for a high gain.



4.3) SECOND STAGE

The second stage of the op-amp acts as a gain stage and to provide enough current to drive a load of 20pF. The compensation capacitor was placed to improve the bandwidth of the amplifier.

Taking parasitic and load capacitance into account, the maximum frequency of the second pole was calculated to be

$$1/RC = gm2/(C1+C2)$$

where C1 and C2 are given from the figure as below

$$C1 = Cgd1 + Cgd3 + Cdb1 + Cdb3 + Cgs5$$

$$C2 = Cc + Cdb5$$

$$C1 = Cc + Cgd5$$

$$gm2 = gm5$$

c1 + c2 can be taken as 20pf as parasitics are negligible as compared to load capacitor
Hence gm2 comes out to be 6.2 mA/V

And from the formula

$$gm = 2I/(Vgs - Vt)$$

I = bias current in second stage is calculated to be 2.3 mA

The 1st pole is arbitrarily chosen to lie at 16Khz

And the 2nd pole is calculated to be 50Mhz

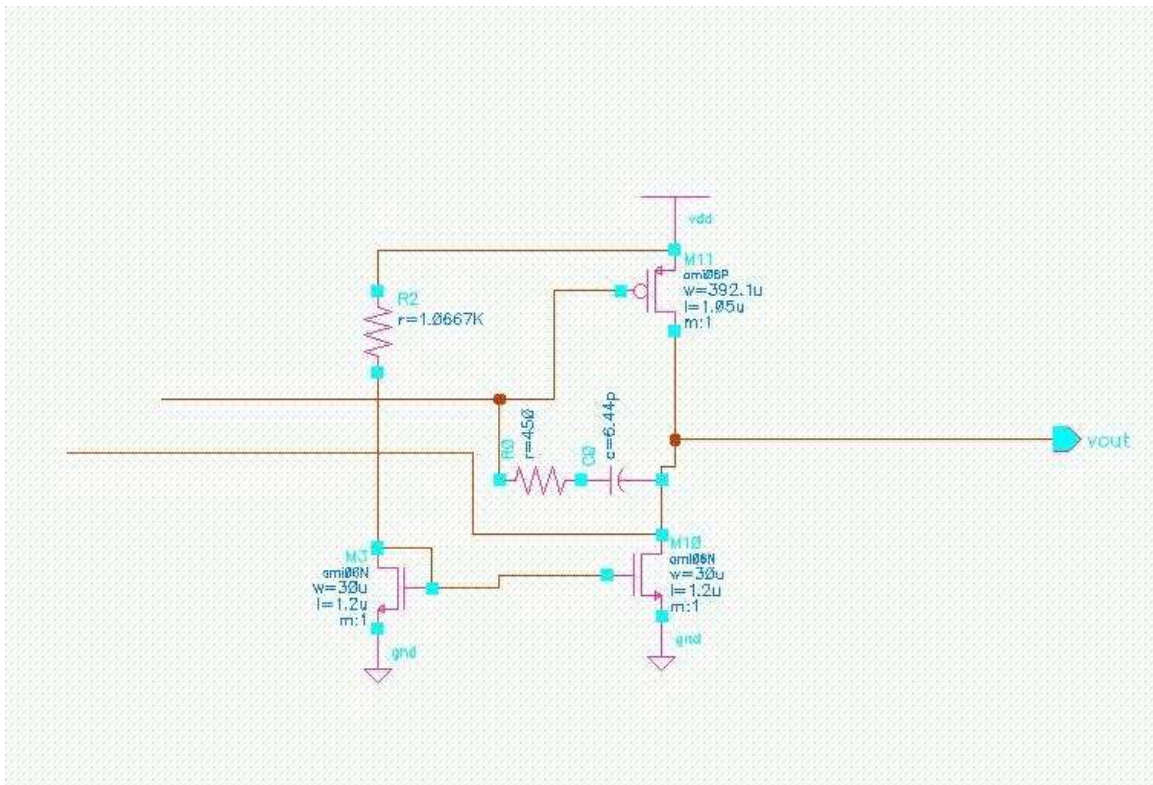
A resistor is placed in series with the capacitor so that the zero does not interfere in the transfer function of the gain.

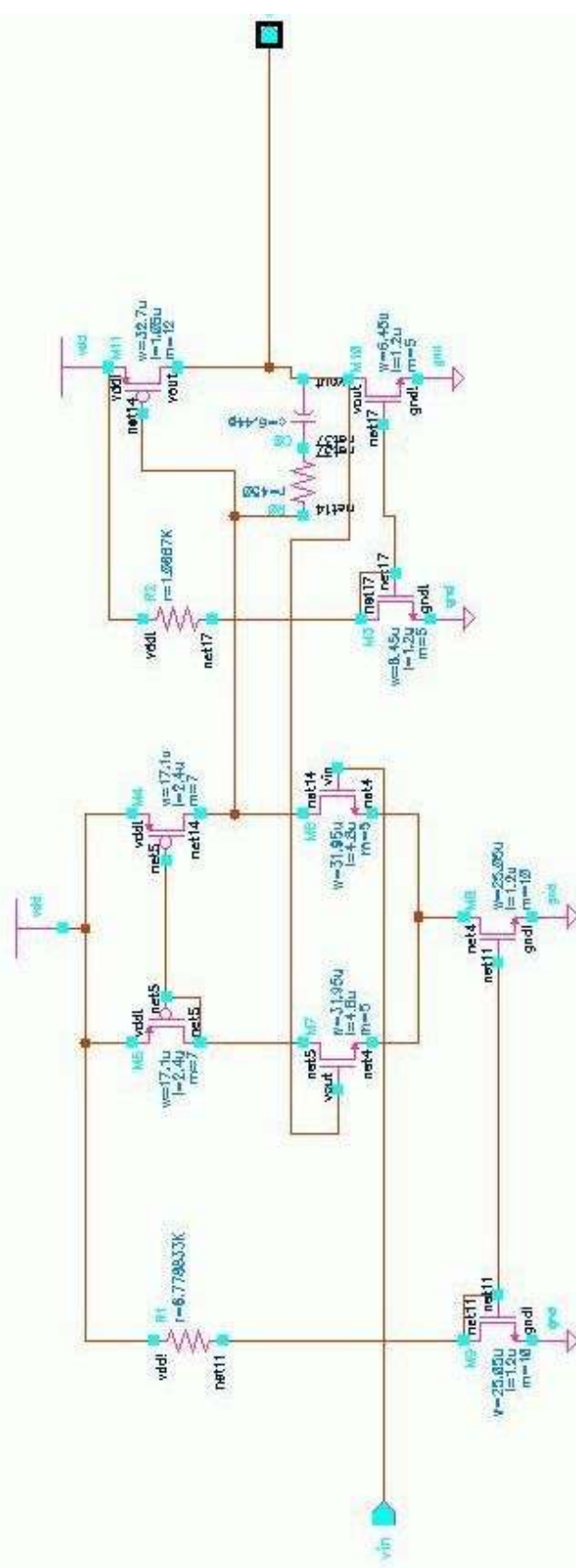
The compensation capacitor is calculated to be 6.44 pF

And the zero resistor is calculated from the formula

$$Rz = (C1 + Cc) / gm5 * Cc$$

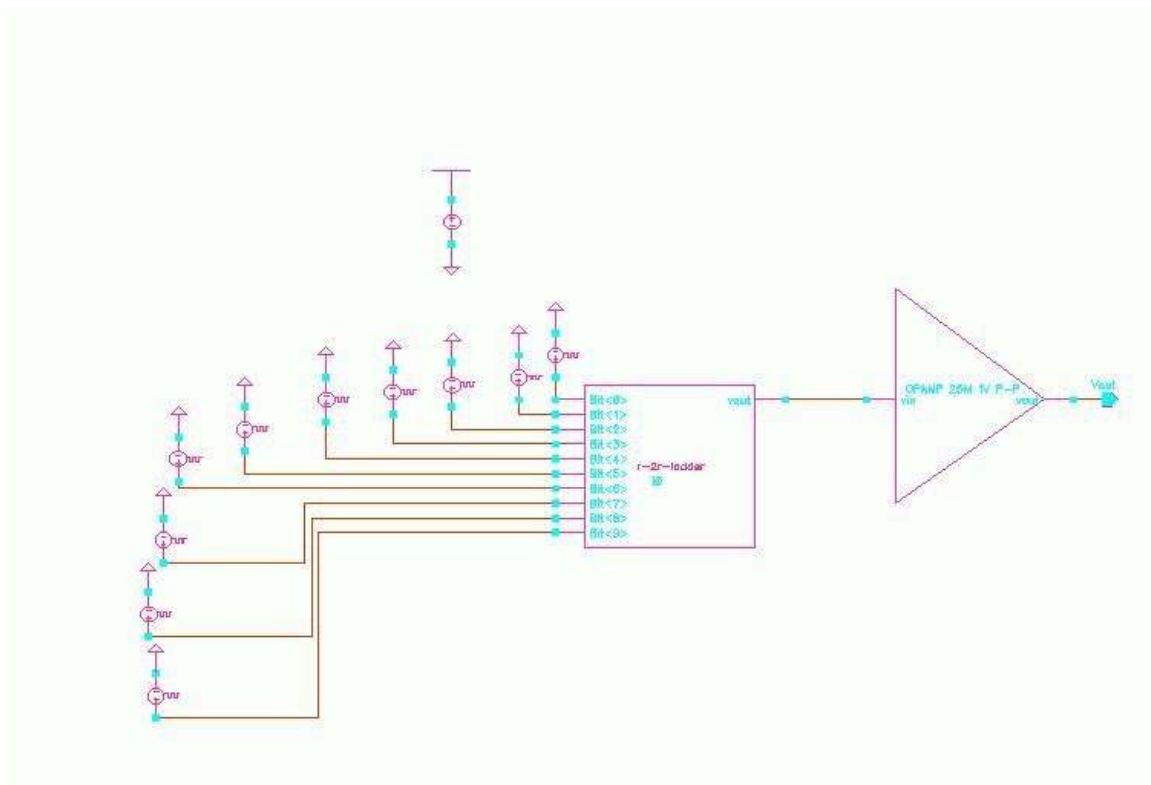
Schematic of the 2nd stage





4.4) DAC

The complete blocks for the DAC is shown in fig below with test circuit to see the DAC works with linearly increasing signal before testing it with the ROM output

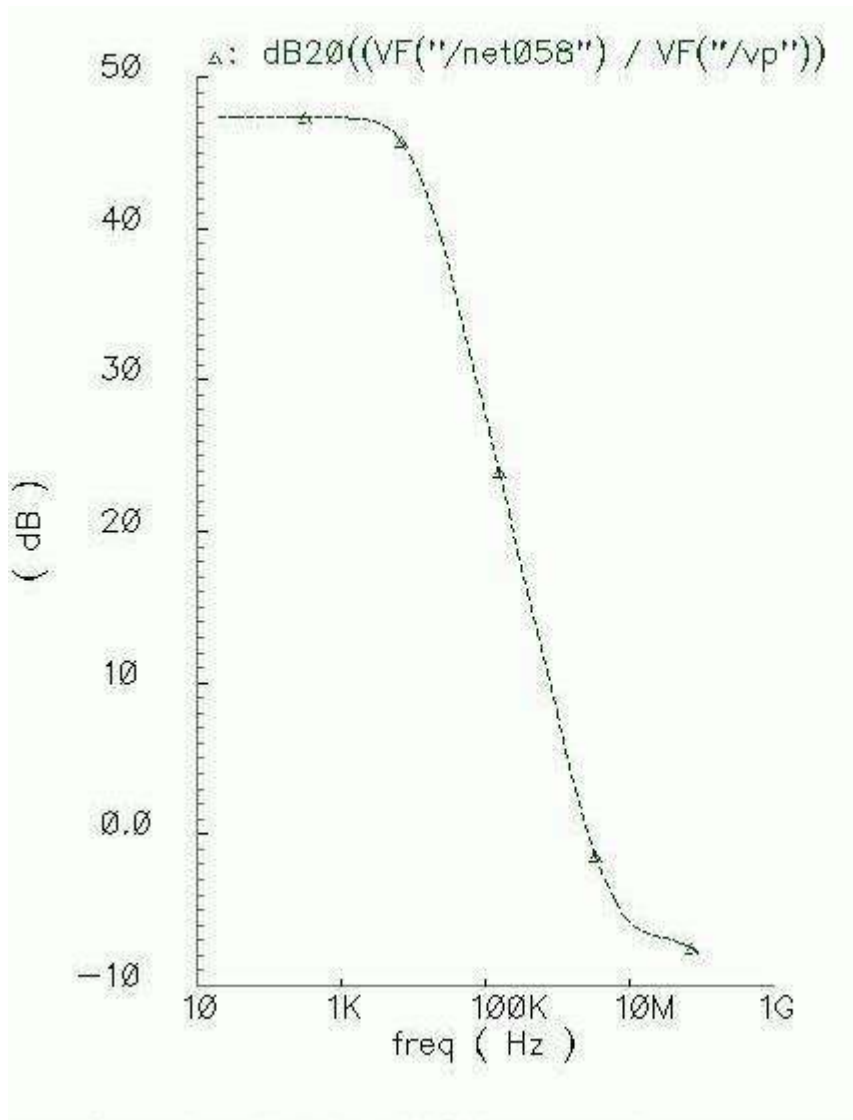


5) SIMULATION RESULTS

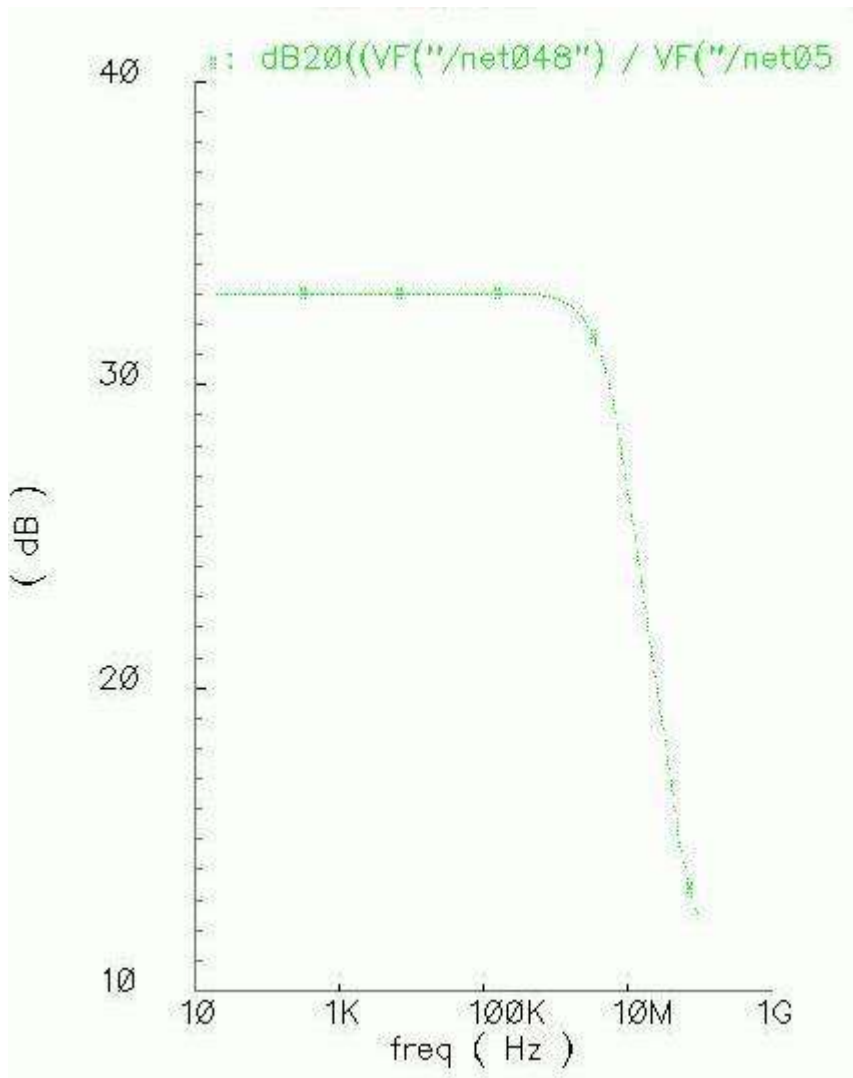
Schematic simulations were performed on all circuits to verify functionality. Simulations with parasitic capacitors extracted from the layout were performed on circuits whose performance was expected to be highly dependent.

All A.C simulations were taken for a frequency range of 100Mhz

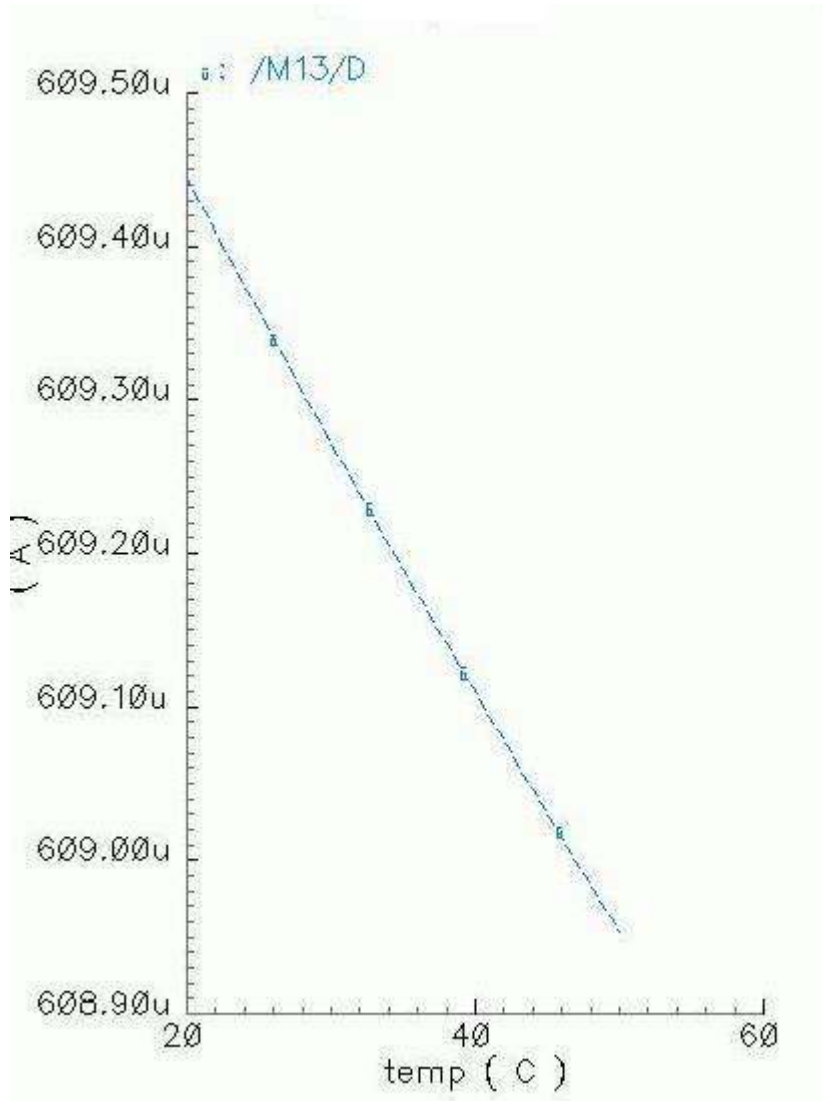
The gain of the 1st stage



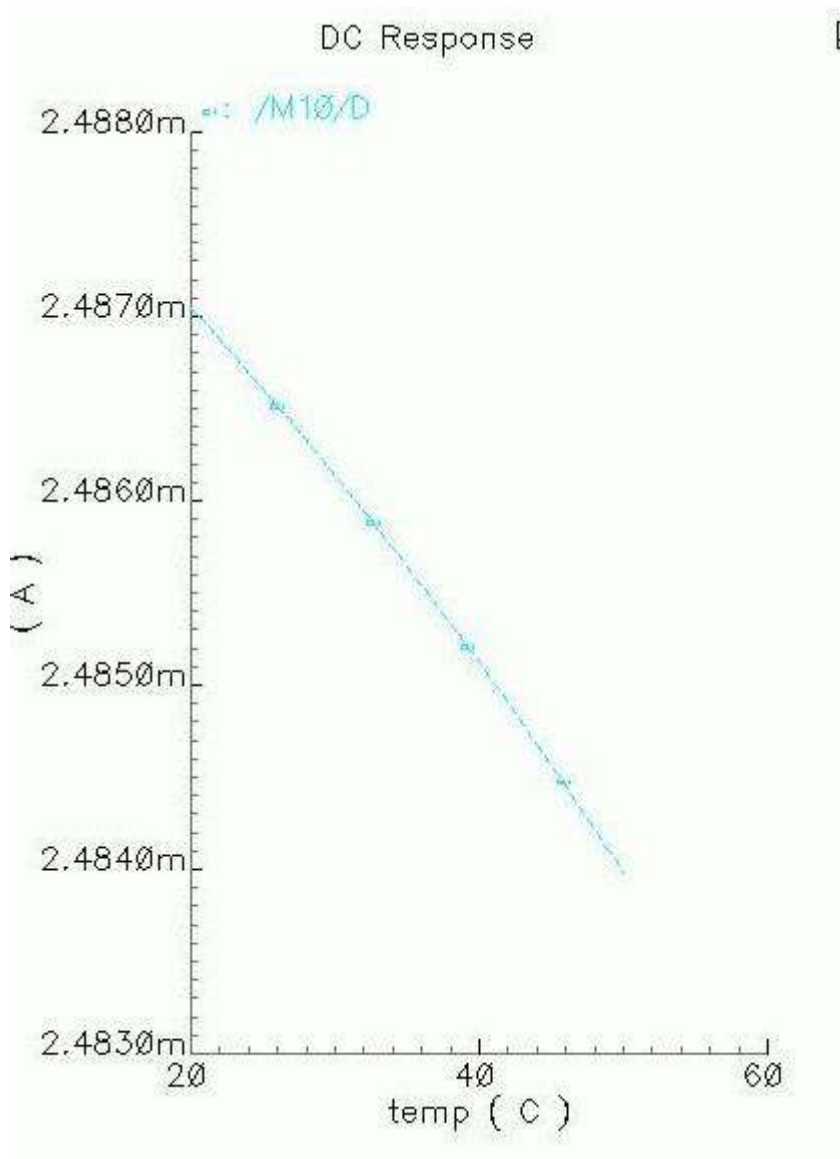
2nd stage gain



DC bias current of 1st stage

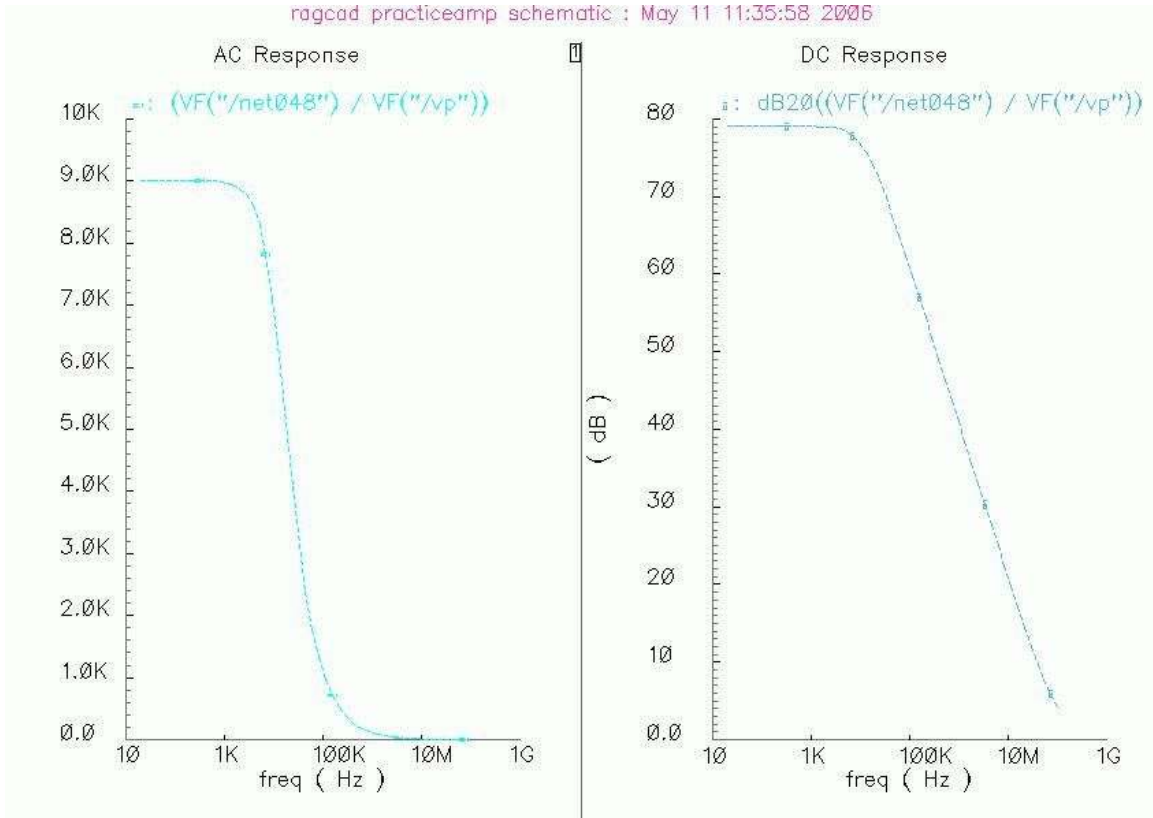


DC bias current of 2nd stage

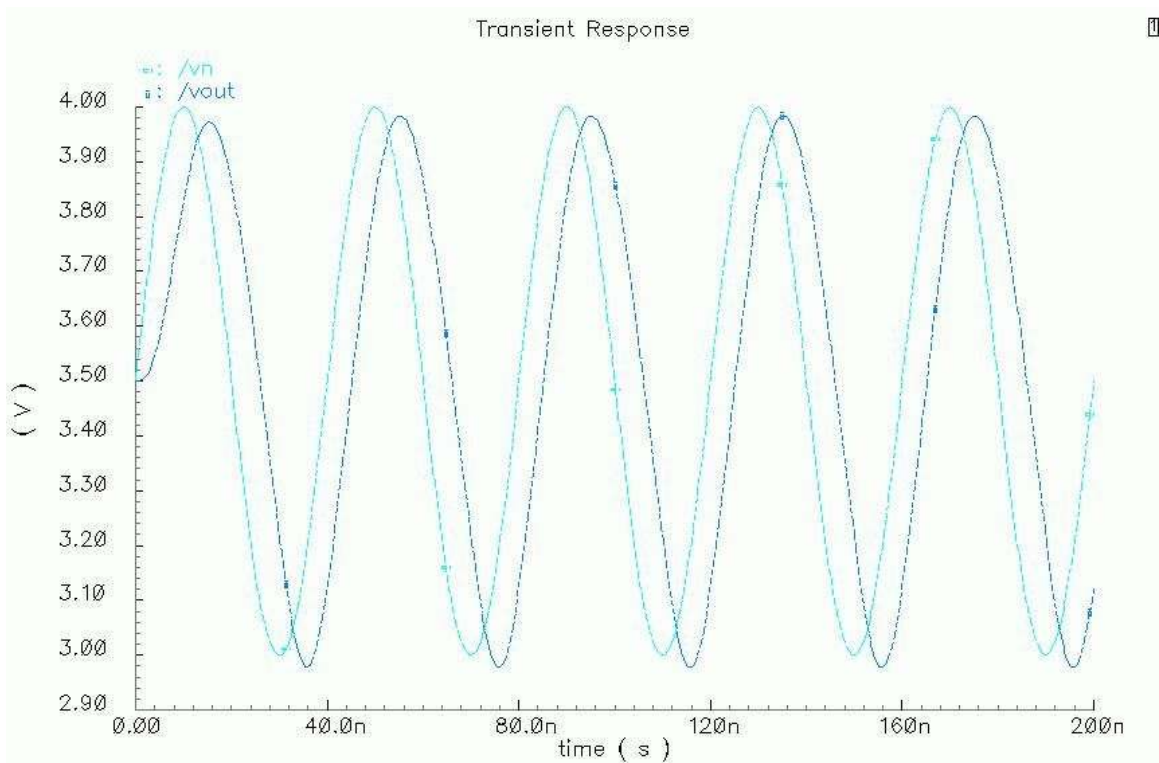


Gain of OP-AMP

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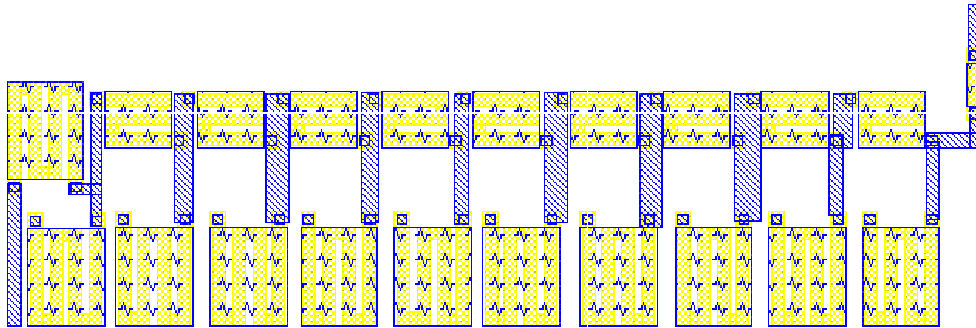
DAC output simulated for a sine wave of 25Mhz



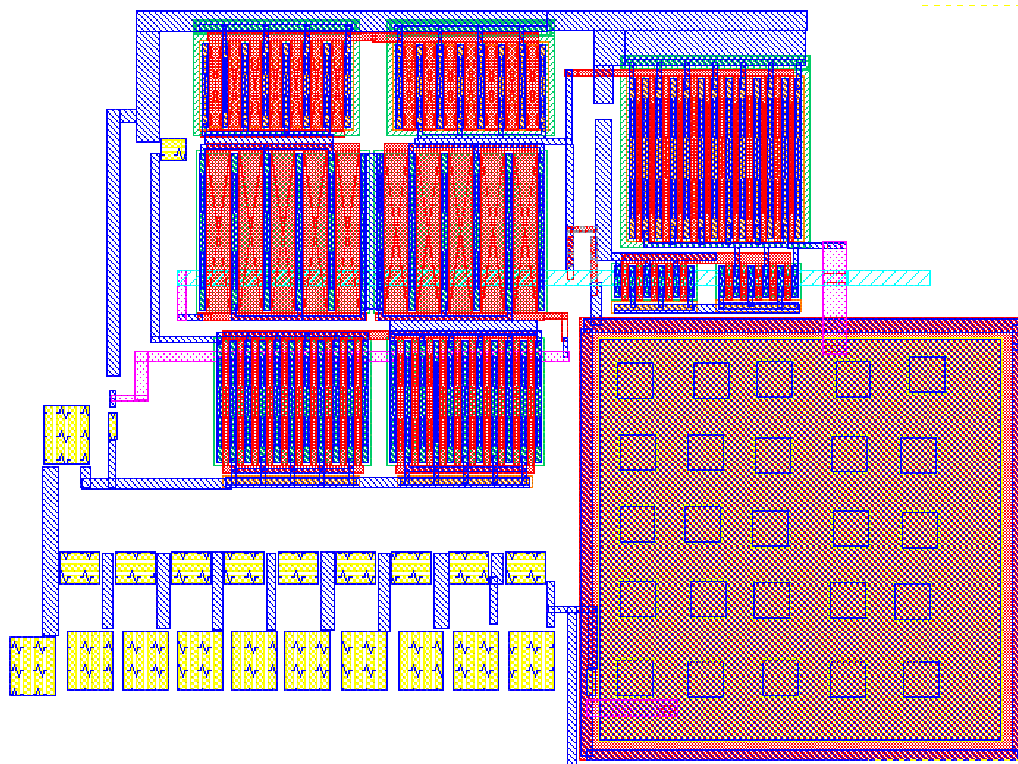
6) LAYOUT DESIGN

The layout for the DAC is shown in the images below in .6um AMI technology. Guard rings of grounded metal 1 to substrate contacts are used to isolate logic components. Supply decoupling capacitors are built in any space not occupied by circuitry.

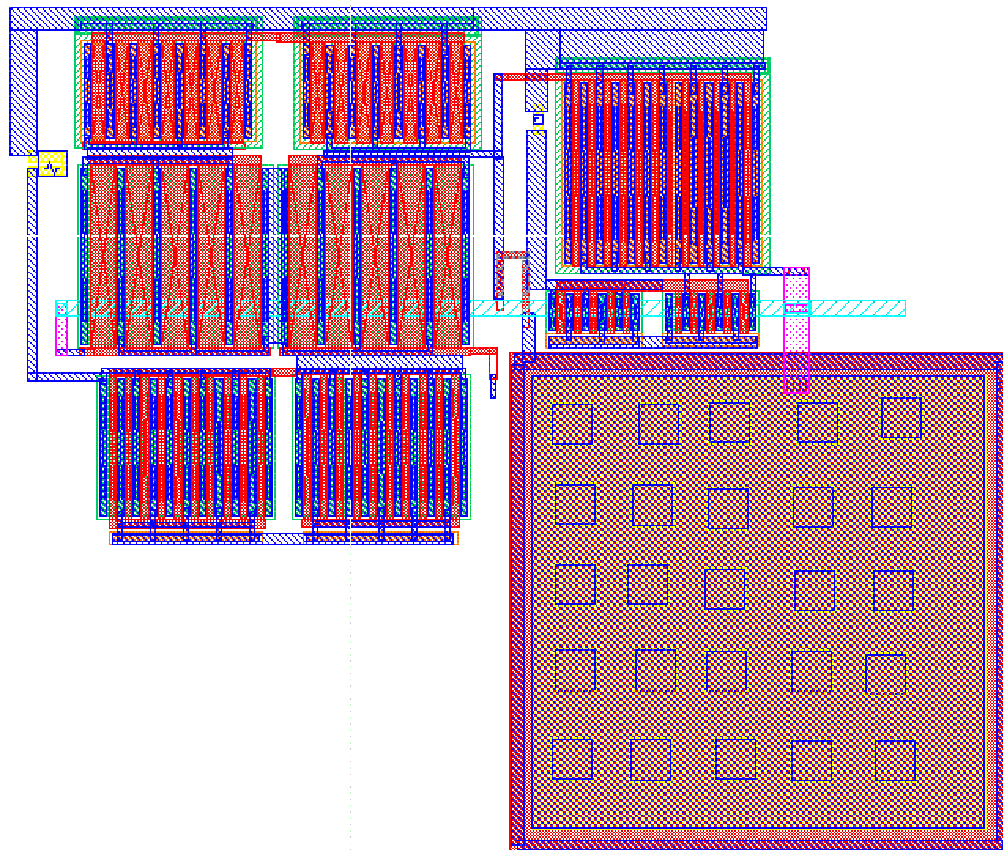
Layout of resistors was done with elec or poly layer.



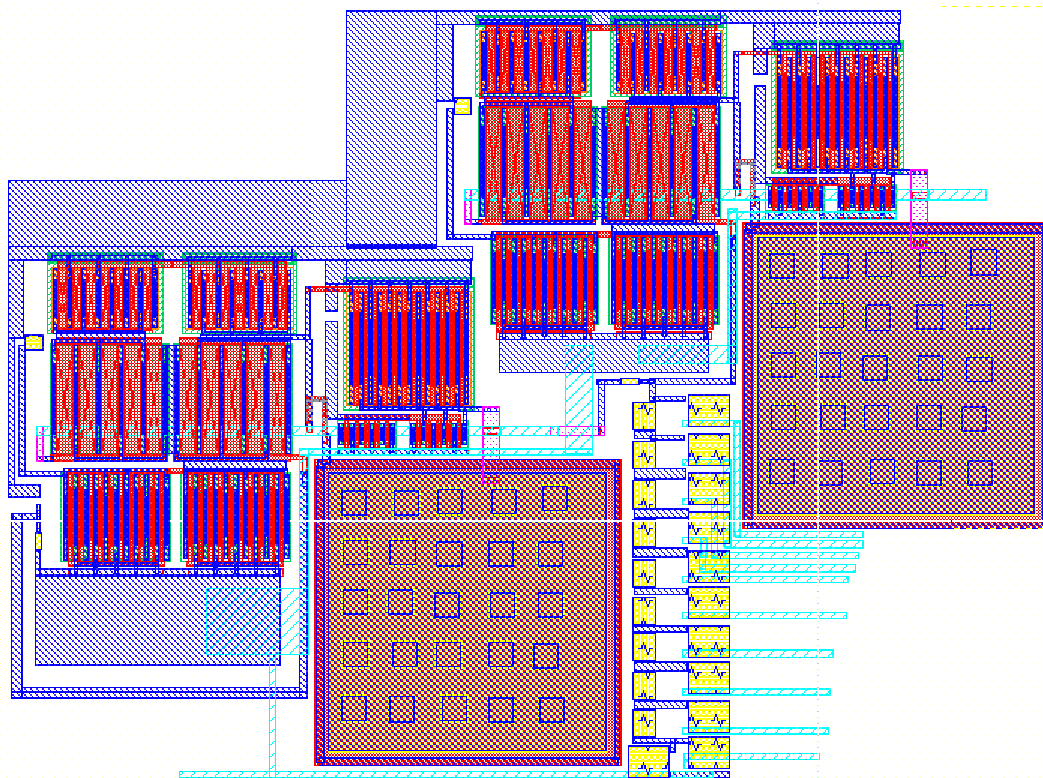
Layout of ladder with buffer shown



Layout of op-amp with compensating capacitor

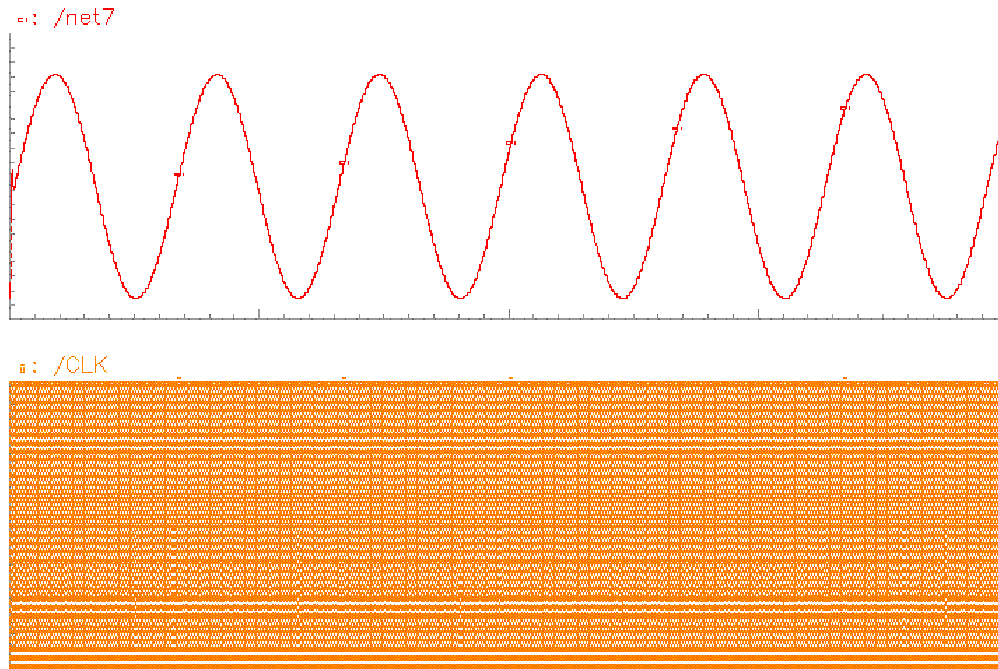


Complete layout of DAC, with 10 inputs fed from ROM



7) FINAL SIMULATION RESULT OF DDS WITH EXTRACTED PARASITICS

The final output simulation with all parasitics extracted and with the output of the ROM connected to the DAC is also shown in the fig below.



REFERENCES

- 1) Design of Analog CMOS Integrated circuits by Behzad Razavi
- 2) www.wikipedia.com