

IR Receiver Demodulator

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ABSTRACT

A revised CMOS design of an IR Receiver demodulator stage, which will reproduce a pulse modulated signal, which will be decoded by a PIC chip. The design is done with the AMI C5N process. The design incorporated improvements that were suggested in the original discrete hardware version made in a capstone project. Simulations show that the circuit accepts a current created by a Infrared photo diode to as low as $.75 \mu\text{A}$, and outputs a 0-5 Volt pulse signal, for which is accepted for use by the PIC chip. The Op-Amps used incorporate a CMOS design, which will allow for high slew rate, and high gain.

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I. INTRODUCTION

A. Project Objectives

This project's objectives is to incorporate the design improvements that were suggested in the Receiver circuit of a capstone project that was made in the previous semester. The Capstone Project was to design an Infrared one-way communication system. The issues of the original design will be discussed in the next section, "Background." The following are the Specifications that will be made for this project:

- Design an Op-Amp that is a single supply
- Have overall project operate at one voltage
- Remove some of the original Op-Amps, to reduce feedback noise
- Incorporate multiple carrier frequency support
- Accept a current input, and output a 0-5 Volt output signal

Incorporating these improvements can remove a diode that will become irrelevant as voltage levels will be purely positive. Which the purpose of the diode is to rectify the signal, due to the PIC chip cannot accept any negative voltage. The original report of the capstone project is available on the website on this project, as a reference.

II. CIRCUIT DESIGN, SIMULATION & LAYOUT

A. Circuit Overview

In the following figure shows the block diagram of the receiver circuit of which this project will be based upon. This project will concentrate on Stages 6 through 9.

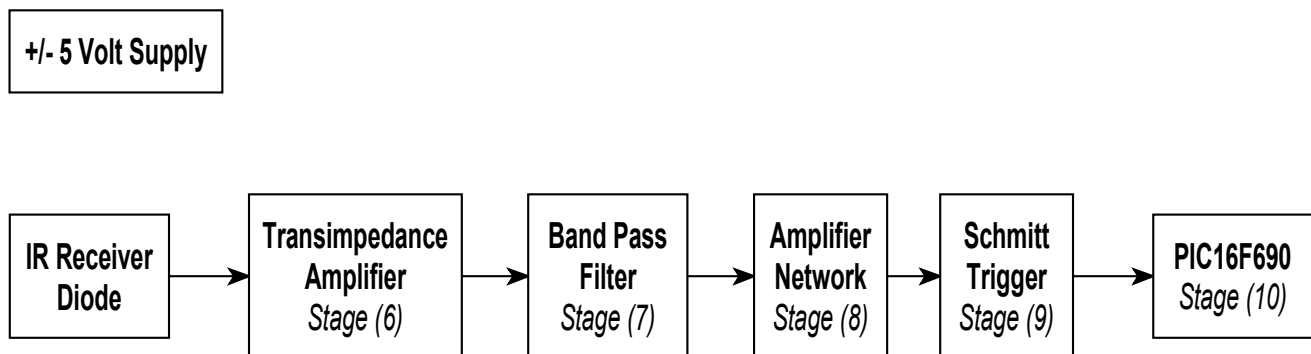


Figure 1. Block Diagram of Receiver Circuit

This section will go into detail on each component, first starting with the components that make

up the Bandpass Filter. The first component discussed is the Op-Amp that was made for this stage, then the resistor networks. Afterwards, the discussion will go from the Bandpass filter (as a whole), the Transimpedance amplifier, Amplifier Network, and then Schmitt Trigger.

B. Op-Amp

As part of the Bandpass filter, it was chosen to use an active filter design. For that, Op-Amps needed to be designed. Figure 2 on the next page shows the schematic of the CMOS Op-Amp that was used in this project. Figure 3 shows the layout of the Op-Amp. Due to the large transistors in the gain component of the Op-Amp, the transistors needed to have multipliers to accommodate for the transistor's need, while having it contained in a small size. The sets of transistors that have a Source-Drain connection, and no other connection, were connected with a fingers configuration.

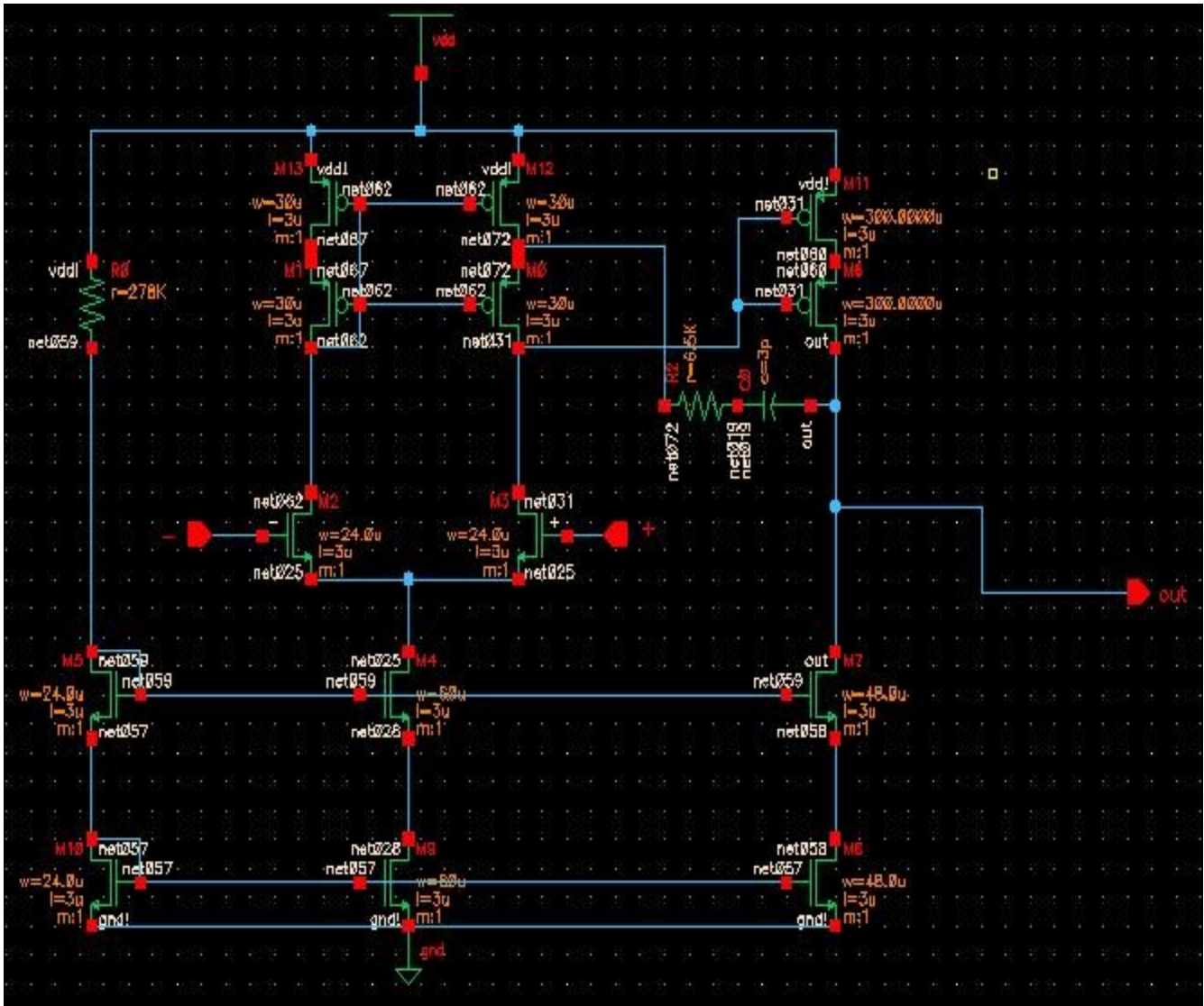


Figure 2: Op-Amp Schematic

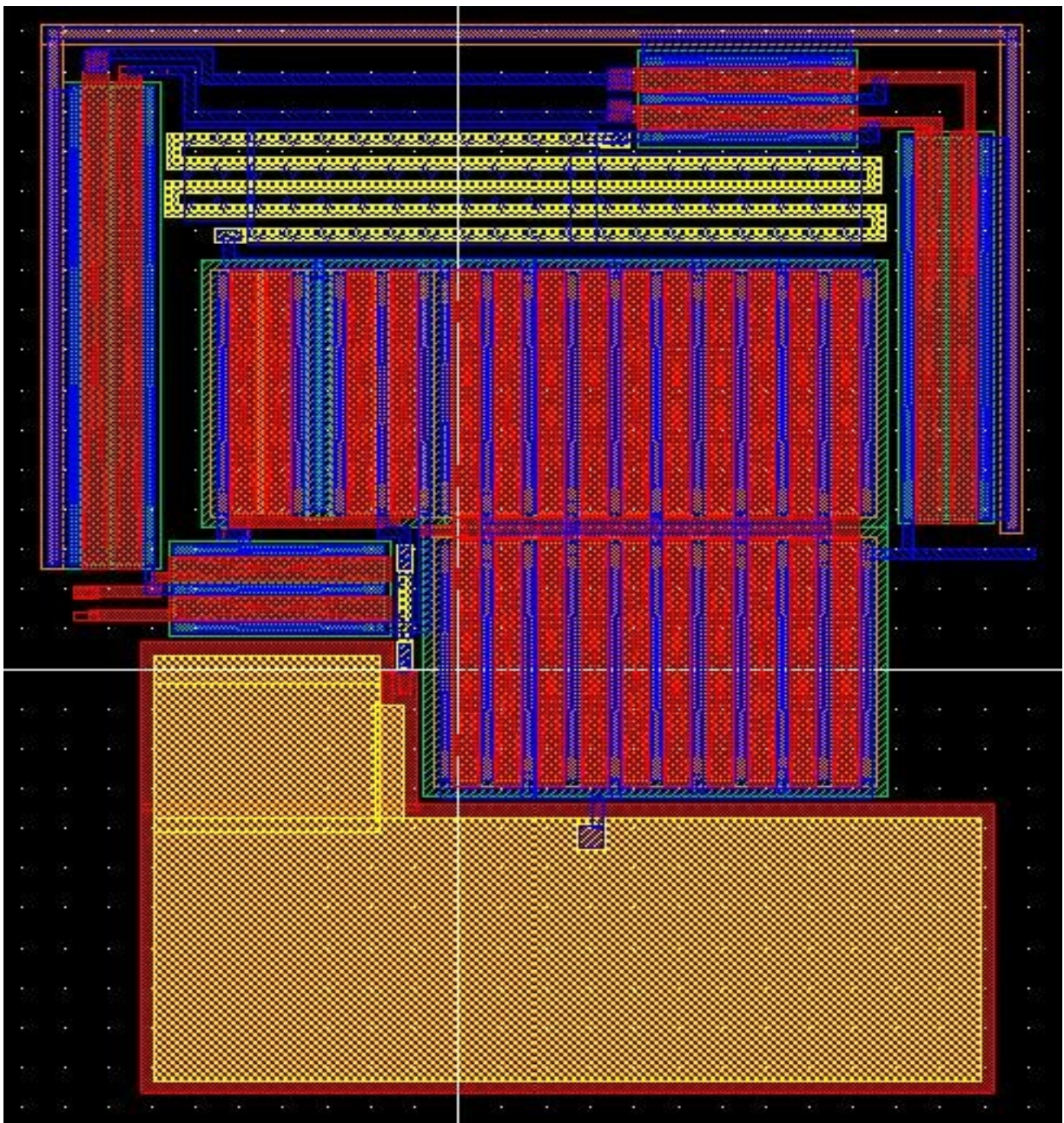


Figure 3: Op-Amp Layout

C. Resistor Network

To accommodate the requirement of supporting multiple carrier frequencies, a filter that has an adjustable bandpass frequency range is required. Rather than creating four bandpass filters each with a different resistor setting, and having a 4:1 Mux to set the filter to be used, the resistors themselves were the ones to be set. First to discuss is the 4:1 Multiplexer, which is the key component of this network.

C.1. 4:1 Multiplexer

A basic 4:1 Multiplexer has two state pins, in which each state pin has a inverted and non-inverting line. The inverters were created with a basic nmos-pmos design. The remaining portion of the Mux contained eight transistors, two per input line. All transistors were minimum size. This design can be seen in Figure 4, the schematic. Figure 5 (next page) shows the layout of the 4:1 Mux. The Table below is the truth table of the 4:1 Mux.

	S1	S2
A	1	1
B	1	0
C	0	1
D	0	0

Table 1: Truth Table for Mux

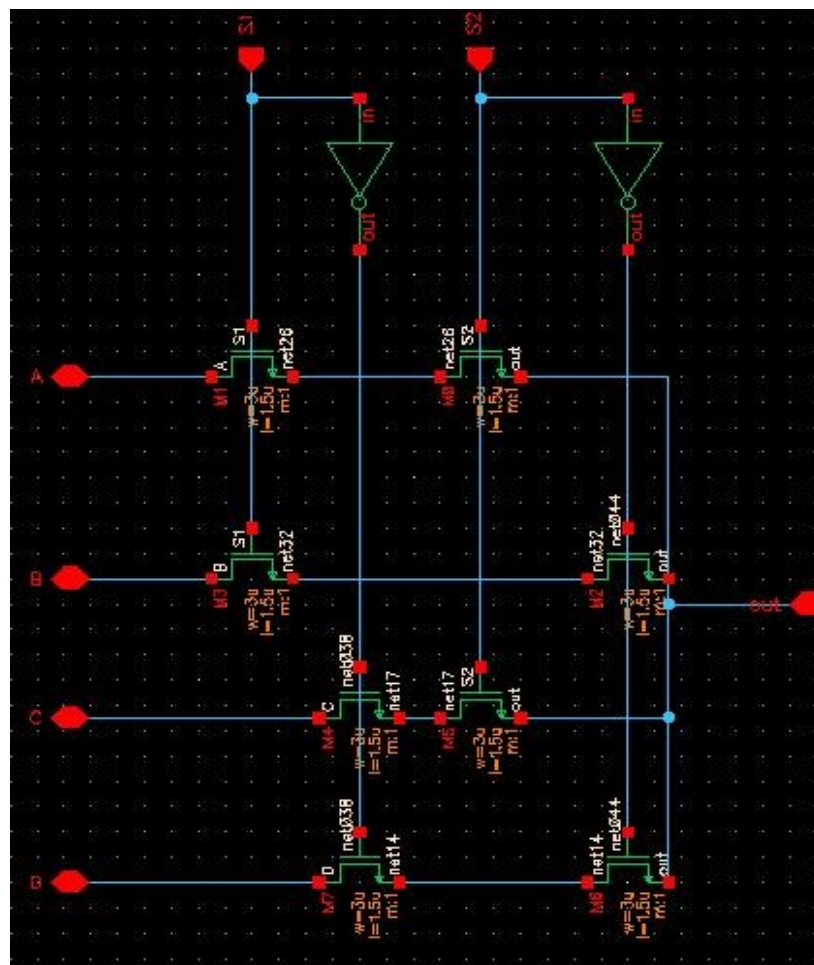


Figure 4: 4:1 Multiplexer Schematic

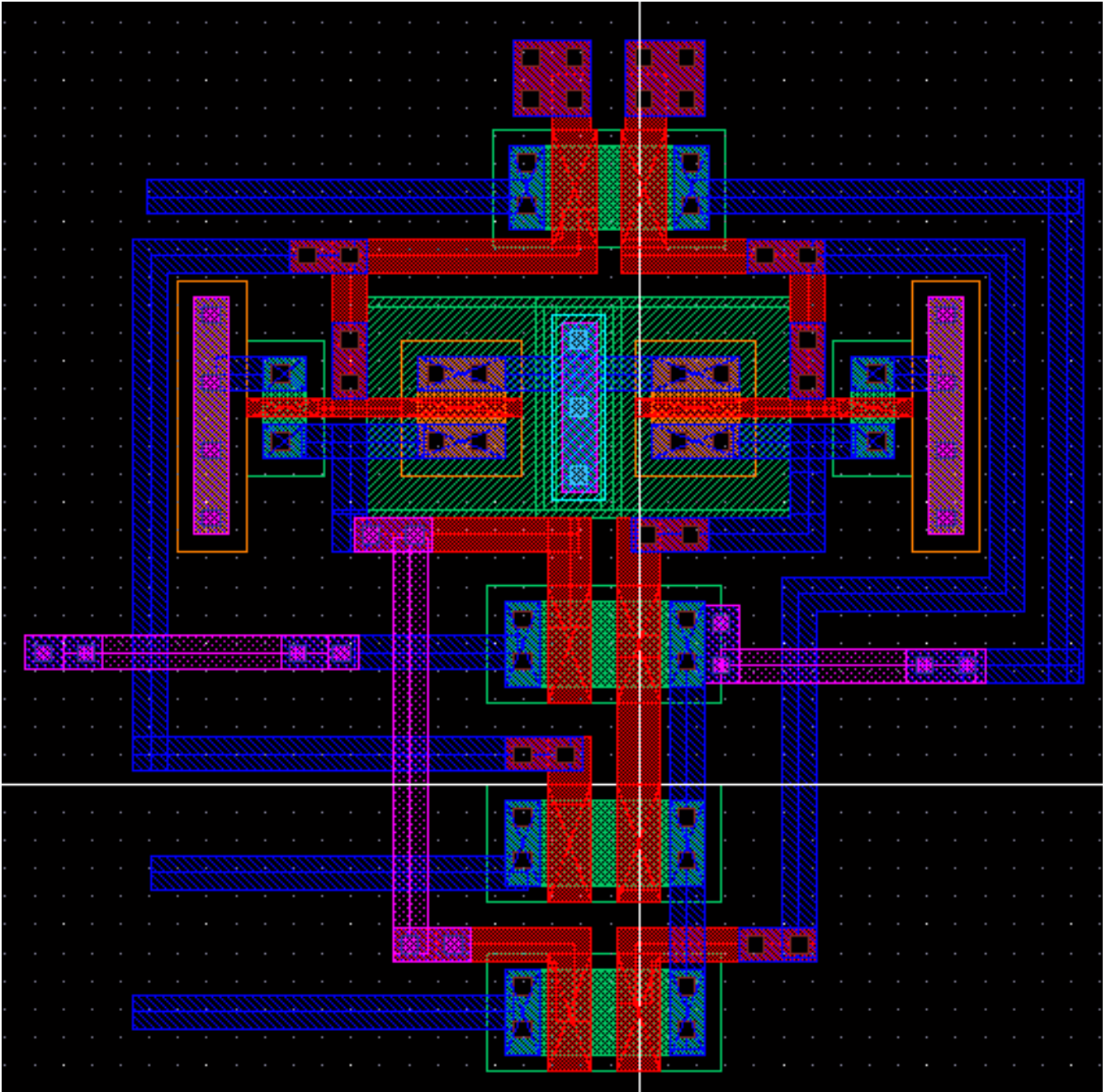


Figure 5: 4:1 Multiplexer Layout

In the layout, terminals on the left go from top to bottom: A, D, B, C; the terminals on the top are S1 and S2 from left to right.

C.2. *Resistors with Multiplexer*

The schematic of the resistor networks are identical, which is basically a resistor tied to each

input, and the the input of the resistors are tied together, as seen in Figure 6. Figure 7 shows the resistor network of the Low Pass Filter, however, the High Pass Filter resistor network is identical in form with larger resistors. The resistors of the networks are in the serpentine form, with a set of equally sized resistors making up a large percentage of each resistor's total resistance.

To determine the resistors used, the carrier frequencies had to be chosen, then offset the frequency by +/-10 Khz, which gives the cut-off frequencies. To set a constant capacitance, the capacitor used was set at 2.4 pF. So with that, the following table (2) shows the math involved to find the resistor values.

State	Transfer Rate	Carrier Freq	low	high	low in rad	high in rad	Resistor low	Resistor High
A	9600	38400	28400	48400	178442.46	304106.17	2335019.7	1370135.53
B	19200	76800	66800	86800	419716.78	545380.48	992732.93	763992.62
C	38400	153600	143600	163600	902265.41	1027929.12	461800.55	405345.72
D	76800	307200	297200	317200	1867362.67	1993026.38	223131.09	209062.29

Table 2: Resistor Value Calculations for Both Networks

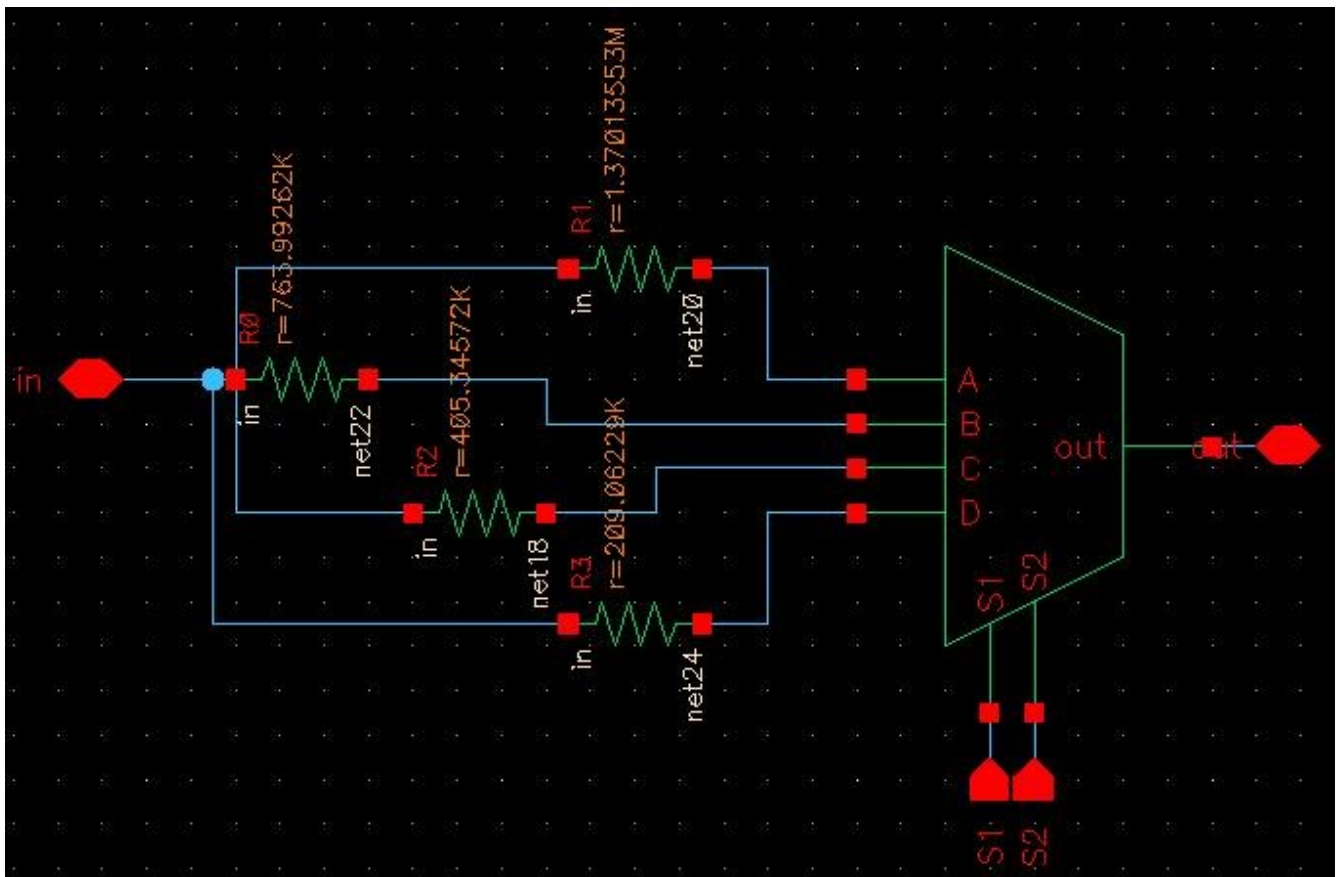


Figure 6: Resistor Network Schematic (Low Pass Shown)

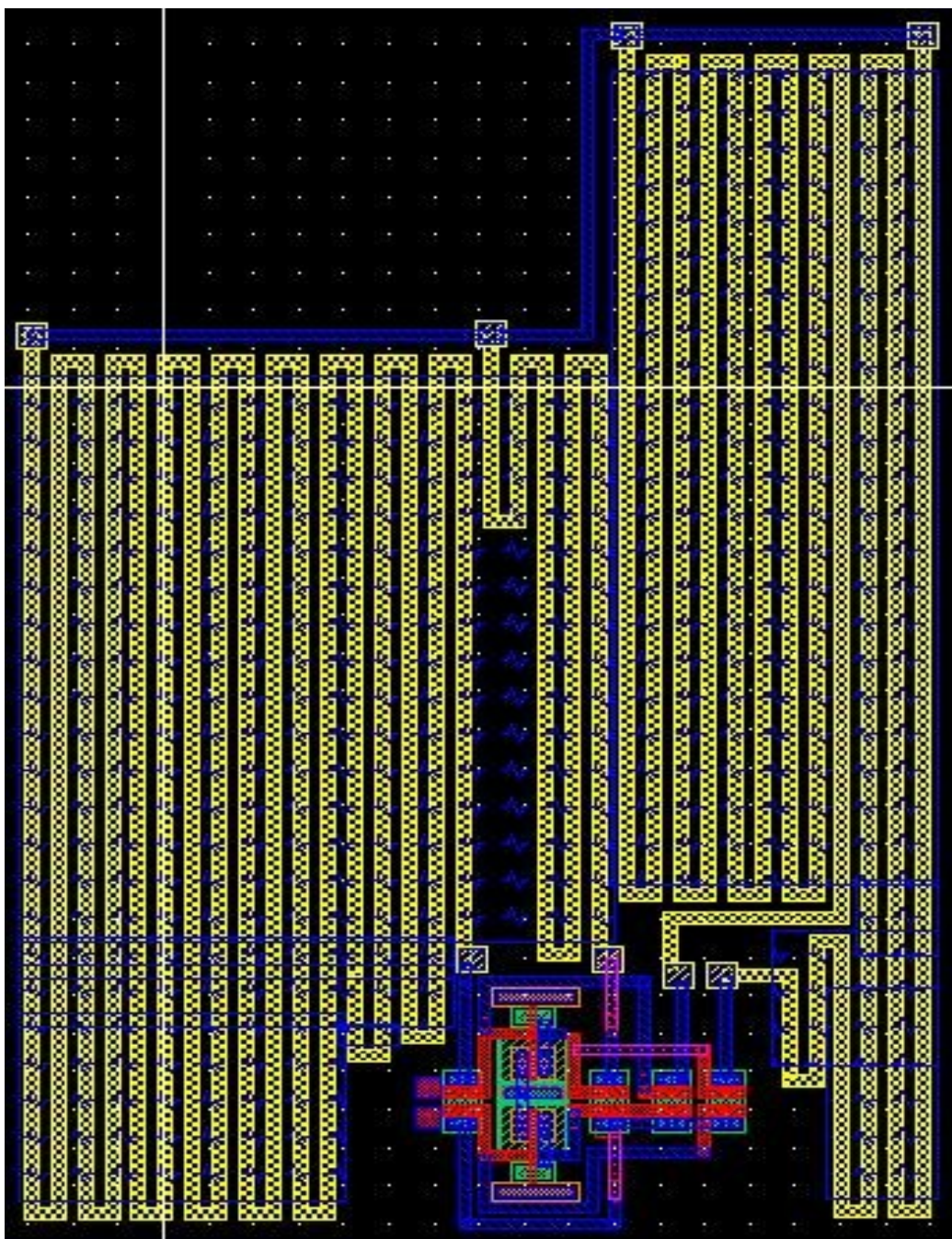


Figure 7: Resistor Network Layout (Low Pass Shown)

D. Bandpass Filter

The band pass filter uses the previously mentioned components to make up the two critical parts of the filters. First to mention, there are more than one way to design this filter, for example, a Butterworth filter could be used instead of a cascade design, which the cascade design is being used here, as shown in the Figure 8 below. Figures 9 and 10 show the schematics of the Low Pass and High Pass Filters respectively. Figures 11 and 12 are the layouts of the respective filters. Lastly, Graph 1 shows the frequency response at all four settings.

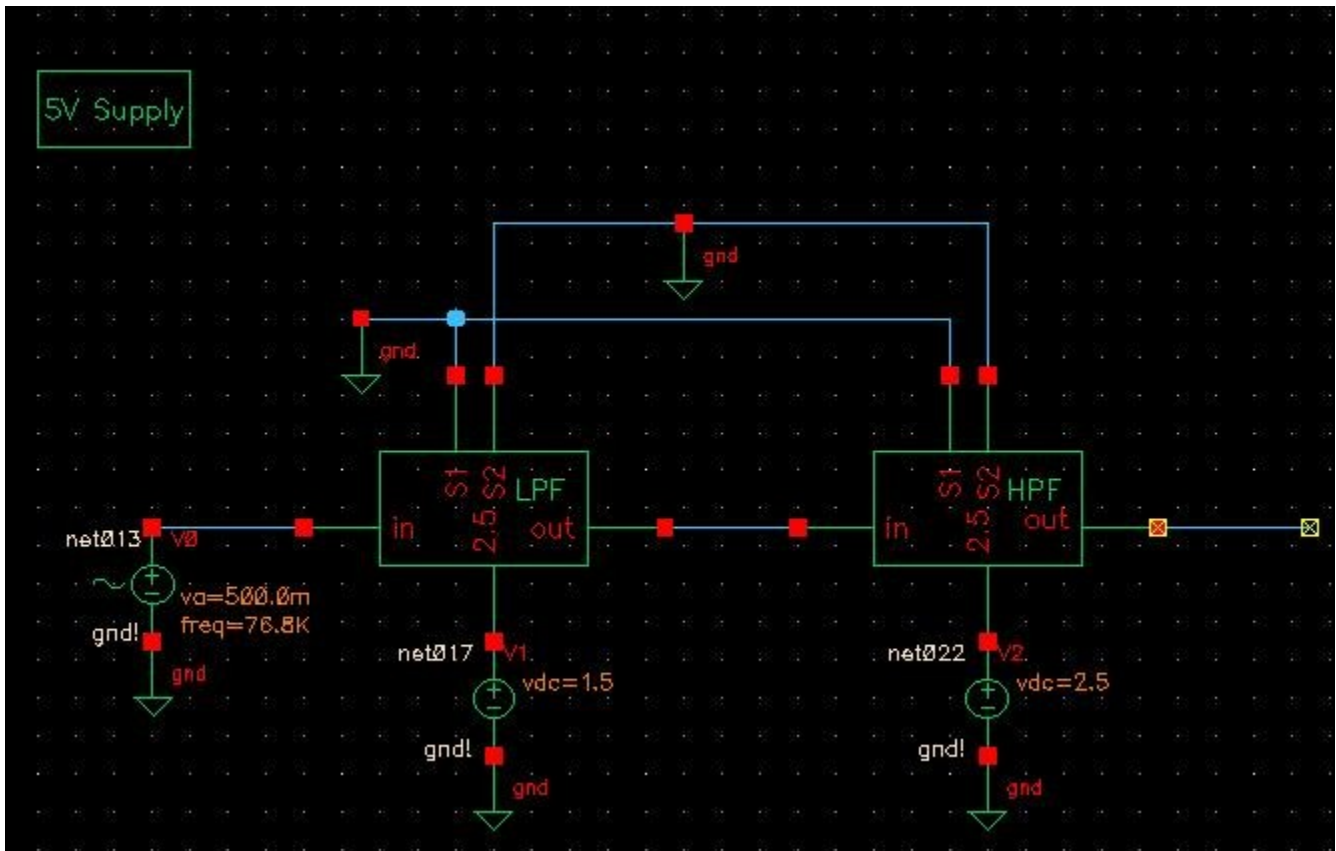


Figure 8: Bandpass Filter Schematic

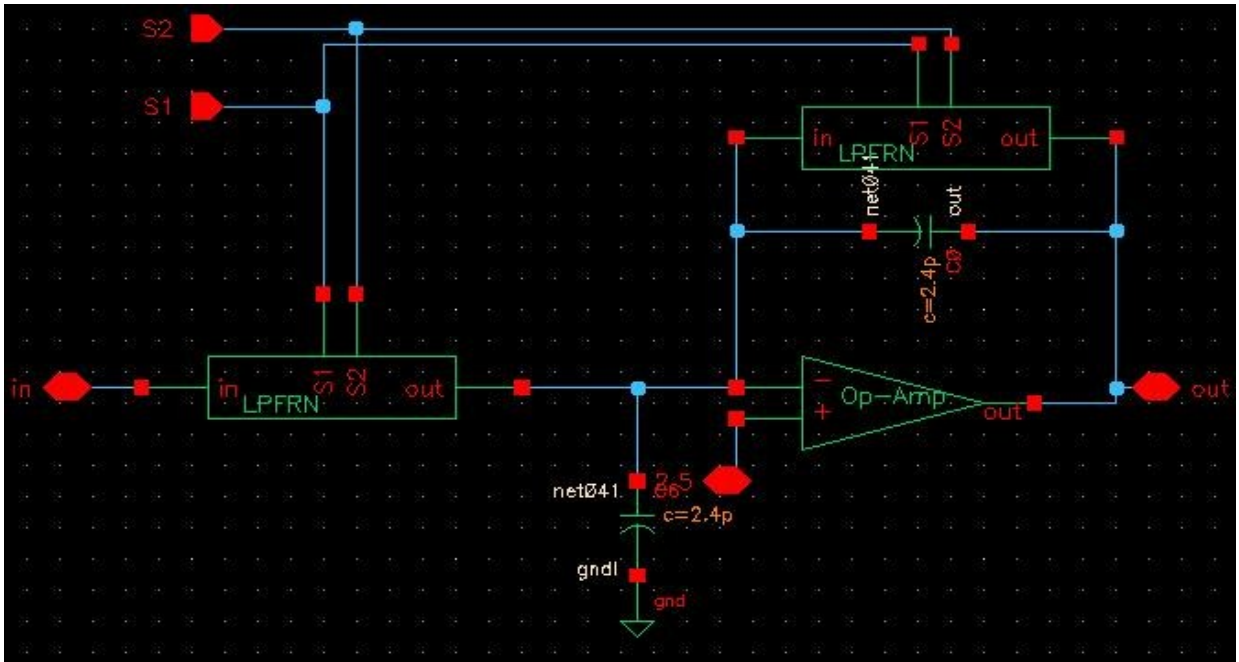


Figure 9: Low Pass Filter Schematic

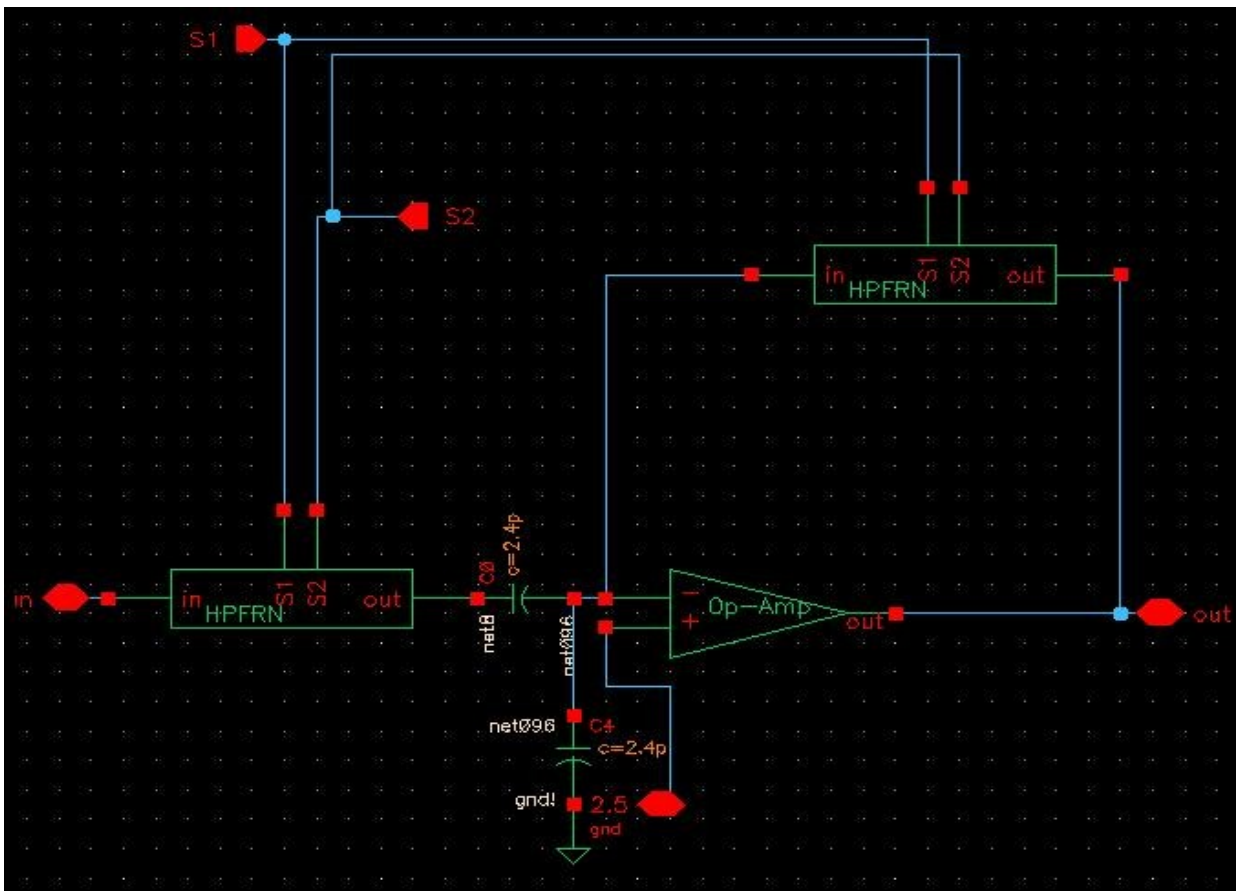


Figure 10: High Pass Filter Schematic

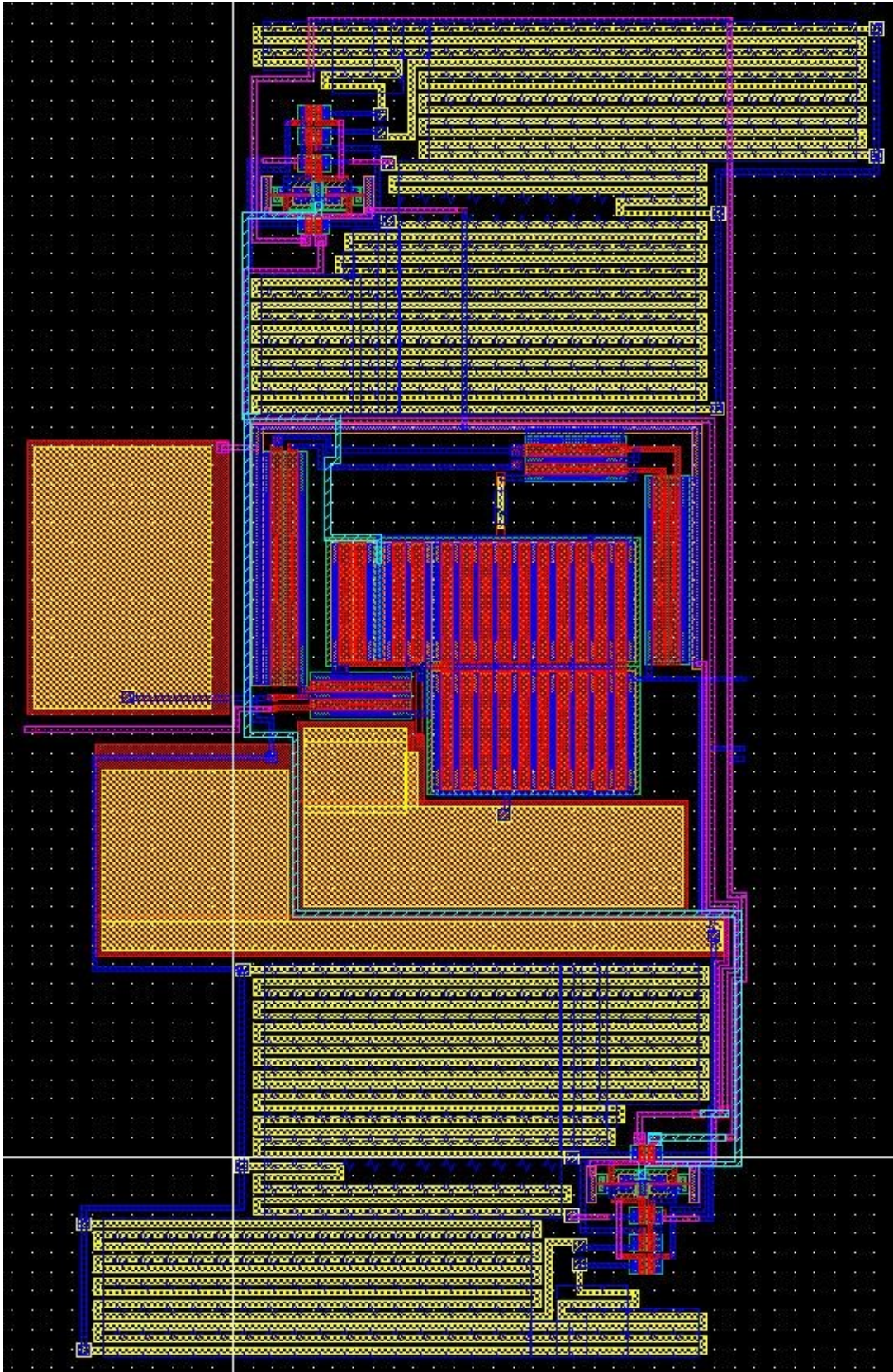


Figure 11: Low Pass Filter Layout

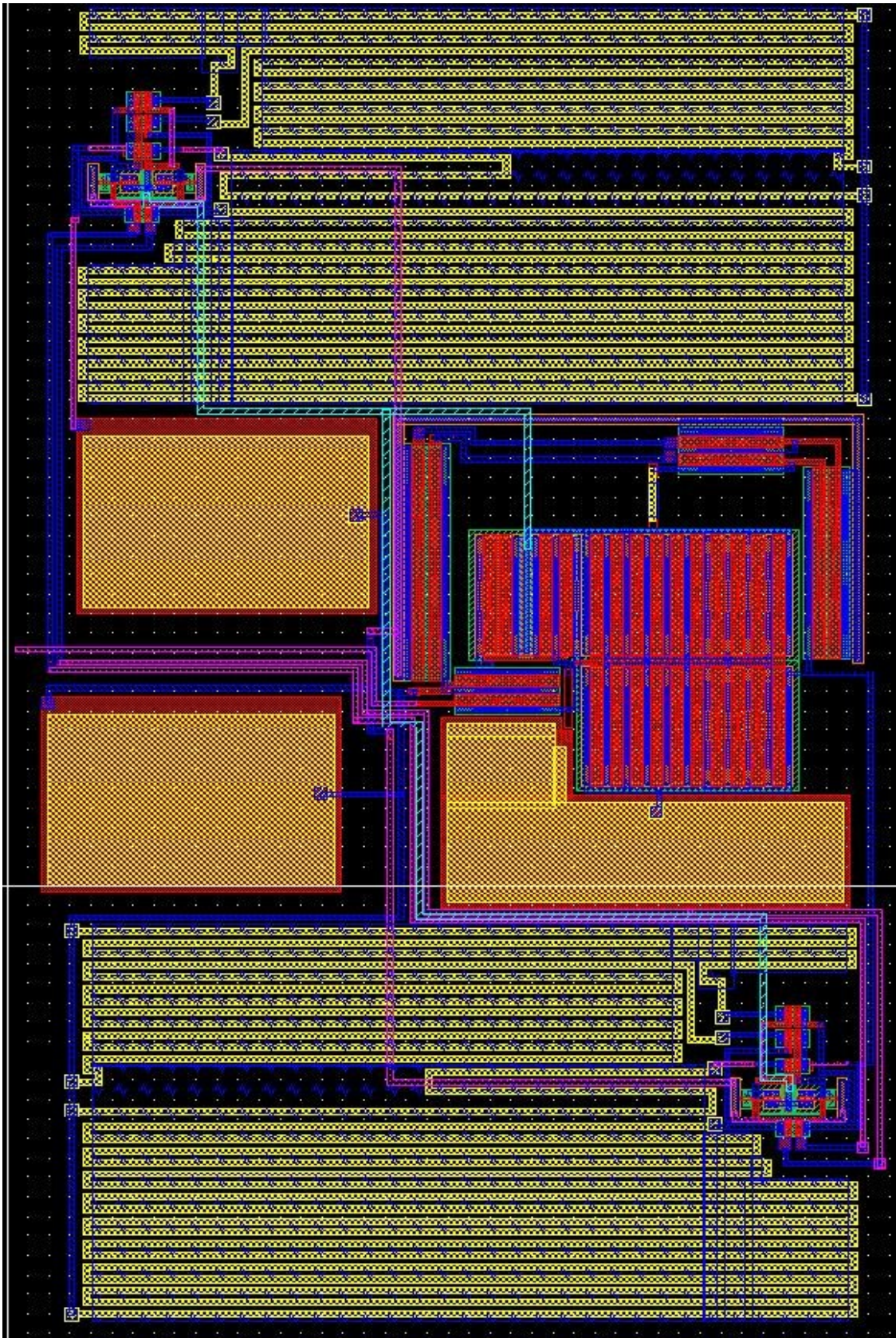
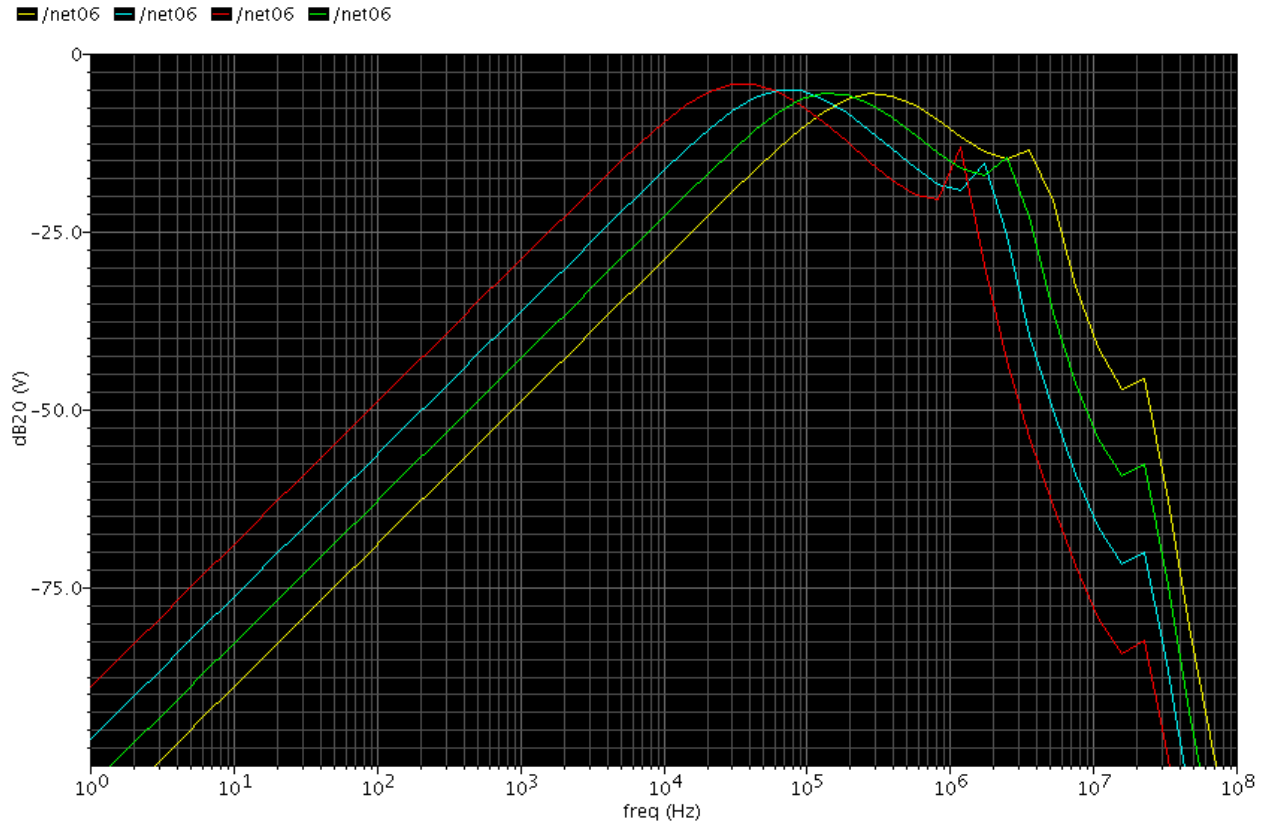


Figure 12: High Pass Filter Layout



Graph 1: Frequency Response of Bandpass Filter

The colors representing:

- Red: S1=1; S2=1; Carrier Frequency= 38.4 KHz
- Cyan: S1=1; S2=0; Carrier Frequency= 76.8 KHz
- Green: S1=0; S2=1; Carrier Frequency= 153.6 KHz
- Yellow: S1=0; S2=0; Carrier Frequency= 307.2 KHz

It should be noted that there is a small attenuation, which is caused by the very narrow bandwidth caused by the cutoff frequencies being only 10 KHz away from the carrier frequency. In the simulations of the complete circuit, it was found that there was also a small oscillation embedded in the signal in the Mhz range, thus a 2.4 pF capacitor was added into the input of each stage to remove to oscillations.

E. Transimpedance Amplifier

As part of the most critical stage, this stage convert the current created by the photo diode, into a voltage, which is useful for the Filter and the later Amplifier stages. The original design used an Op-Amp. This time there is a transistor design, which includes a long-channel biasing circuit.

E.1. Biasing Circuit

The design was taken from the text book¹, in which also requires a biasing circuit for some of the transistors. Due to the process having a minimum gate length of .6 micron, the design was chosen to be in long channel form. The biasing circuit was also gathered from the text book¹ also. Figure 13 shows the schematic. Graph 2 shows the simulation results, in which the order of the voltages are from top to bottom: Vbias1, Vbias2, Vbias3, and Vbias4. It is also shown what are the values of each output. It is noted that “Vbias4” is not used anywhere in the circuit, however the schematic and layout (Figure 14) both accommodate for the voltage, in case of another design that may use it.

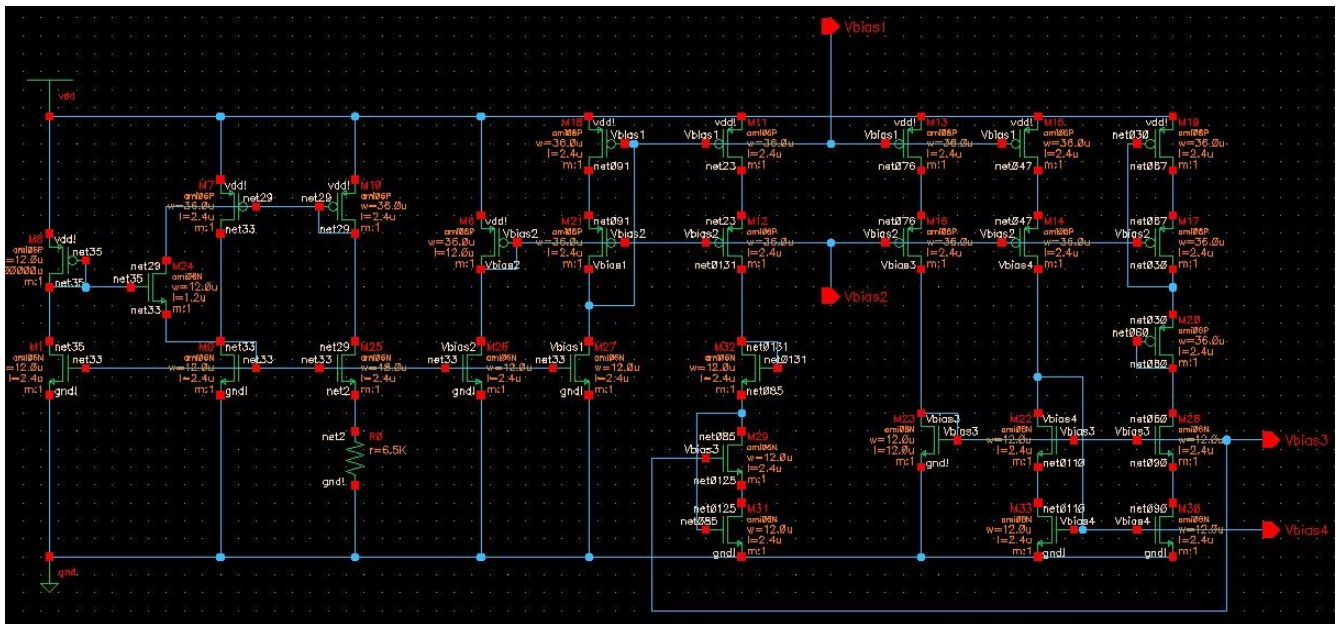
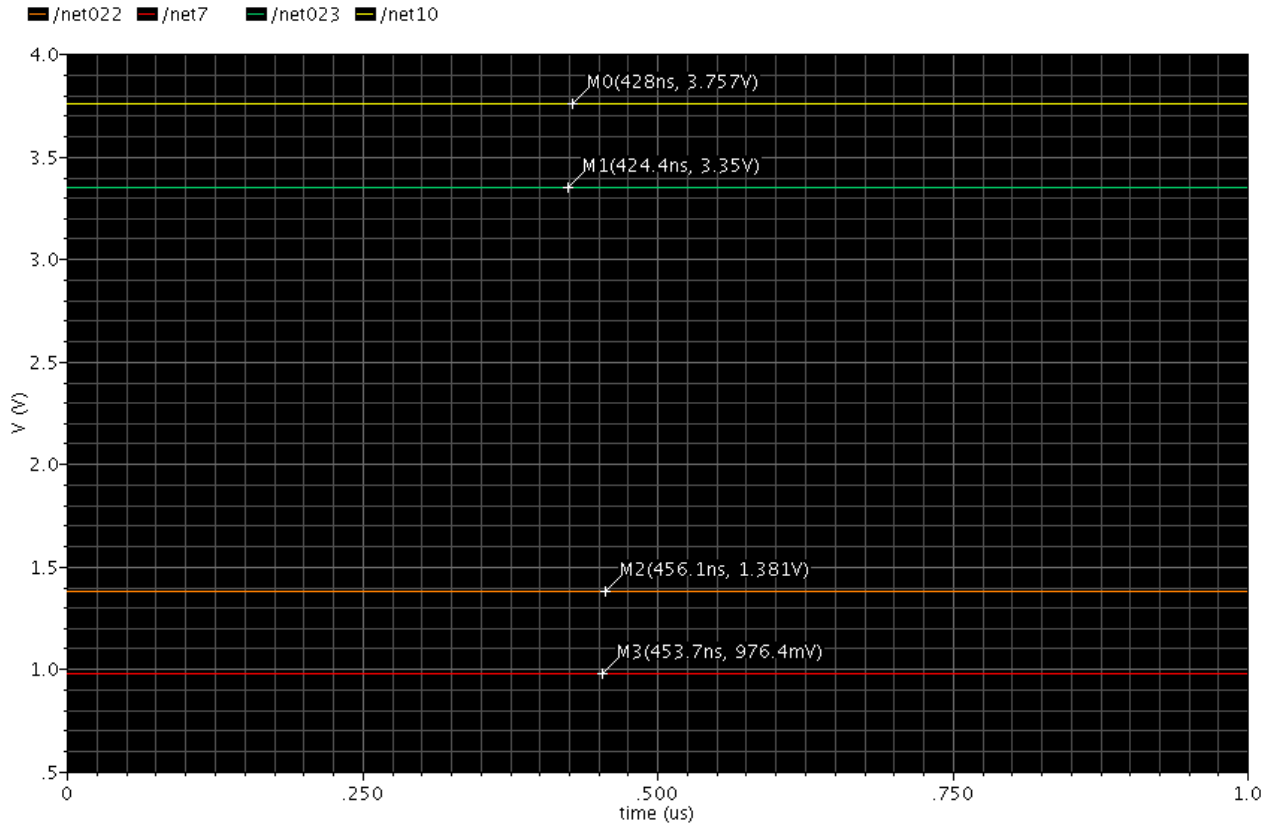


Figure 13: Biasing Schematic



Graph 2: Biasing Voltage Levels Simulation

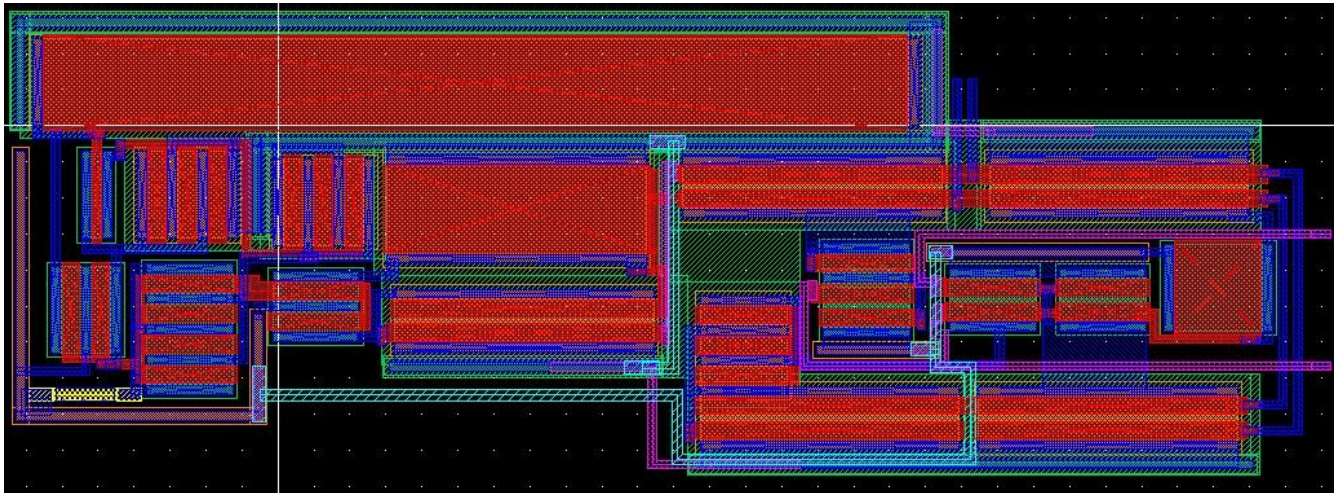


Figure 14: Biasing Layout

The pins on the top right start from the left pin to the right: Vbias2, Vbias1, Vbias4, Vbias3.

E.2. Transimpedance Amplifier

Using the biasing circuit from the previous section, the schematic from the text book¹ was applied. The circuit does require a large capacitor and resistor, which was chosen to be external to the chip. There was noise that was created in initial simulations, which was solved by placing a 1 pF capacitor parallel to the resistor, and unlike the resistor, the 1pF capacitor was placed internally. The capacitor and resistor used external to the chip are 6nF and 10M Ω respectively. The connections will be shown in chip connection layout.

The following figures show the schematic (Figure 15), simulation (Graph 3), and layout (Figure 16). The schematic and layout both incorporate the biasing circuit automatically.

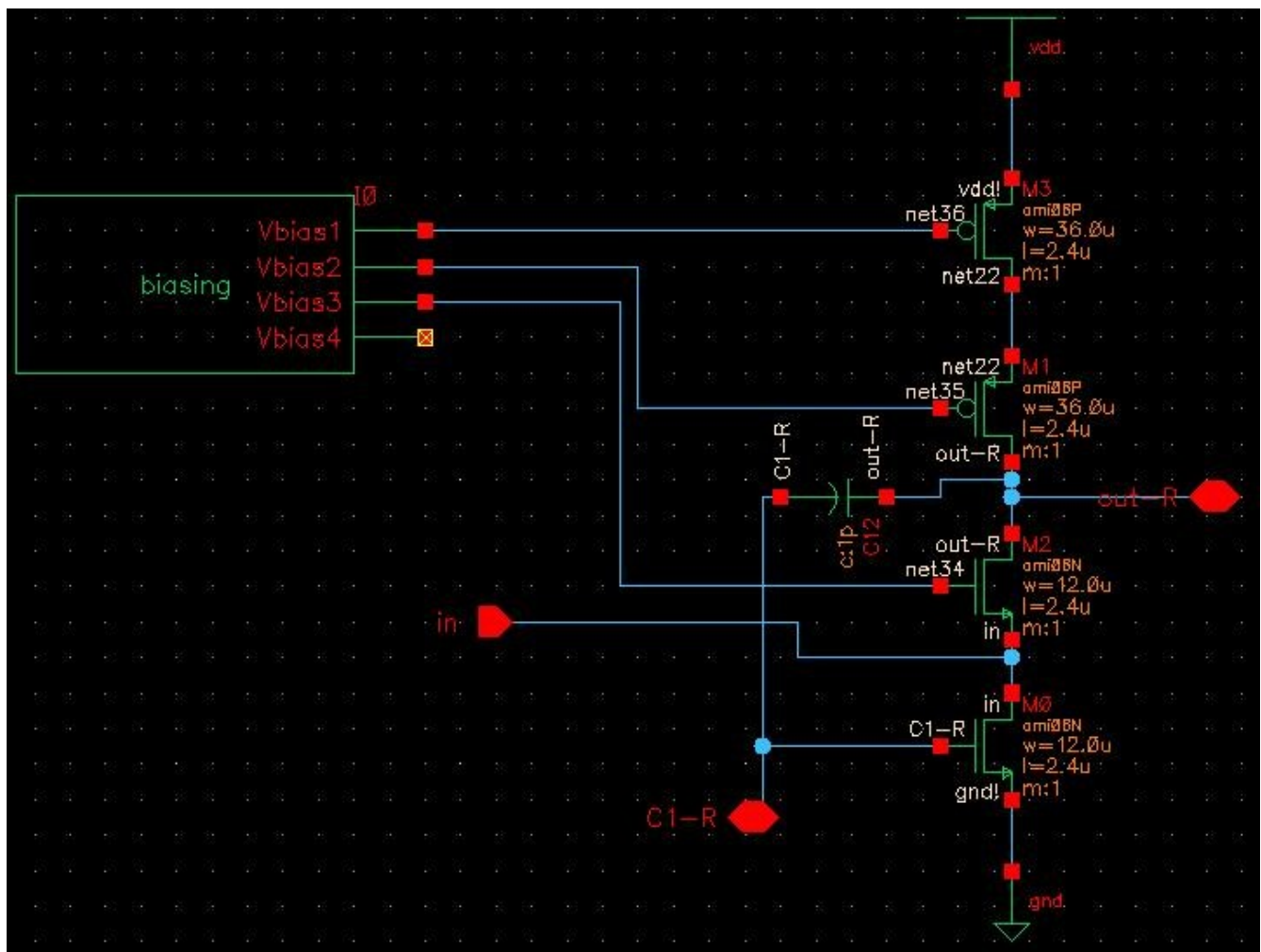
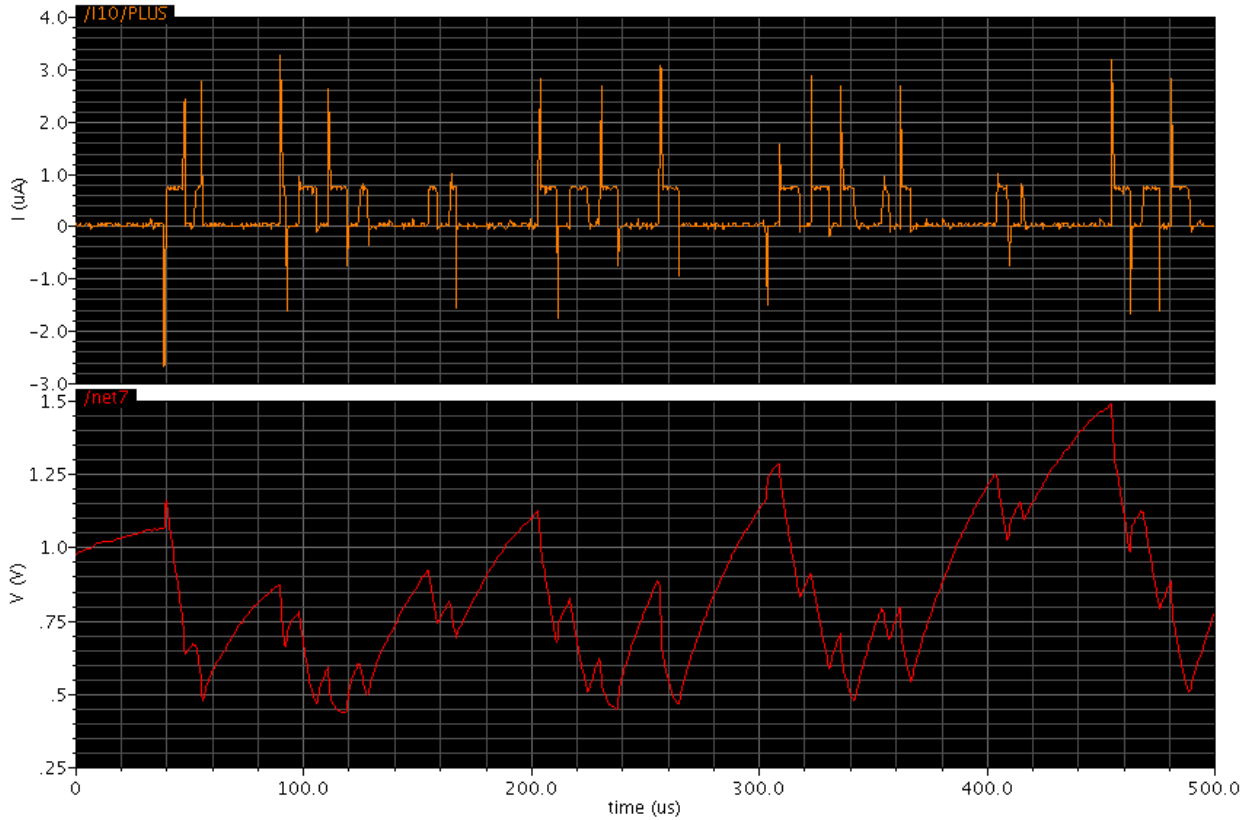


Figure 15: Transimpedance Amplifier Schematic



Graph 3: Input and Output of Amplifier Simulation

In the simulation above, the upper graph is the input current while the lower is the output voltage. This is shown as a comparison of the structure and propagation delay. The result is inverted, which is expected as the gain is equal to $-R_{ocas}$.

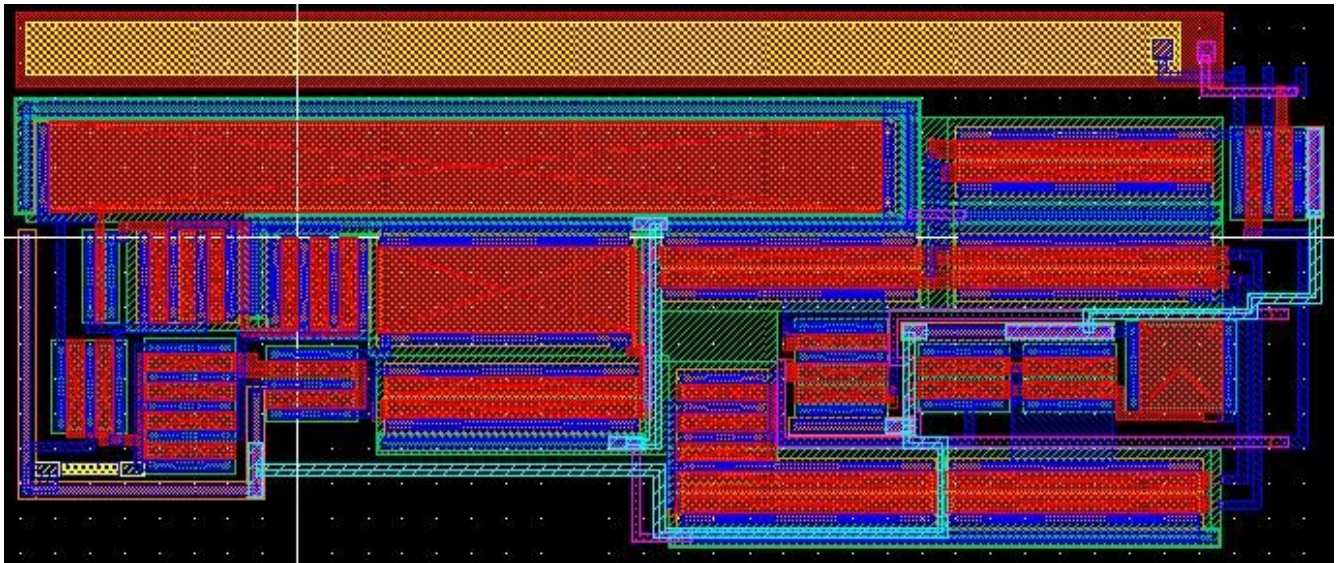


Figure 16: Transimpedance Amplifier Layout

F. Amplifier

The purpose of this stage is to amplify the signal to to such a point that the Schmitt Trigger can trigger the output to a 0-5 Volt pulse signal, which is what is desired. This design uses a non-inverting Op-Amp amplifier stage. At first the gain was set to 21 V/V. With a Schmitt Trigger set with thresholds at 2.45 and 2.55 Volts, simulations produced no results. So the gain was increased until the correct response was shown, which was 51 V/V, or 34 dB, which is shown in Graph 4. Figure 17 has the schematic, which also incorporate the correct biasing for proper operations (net 2.5). Figure 18 has the layout of the amplifier.

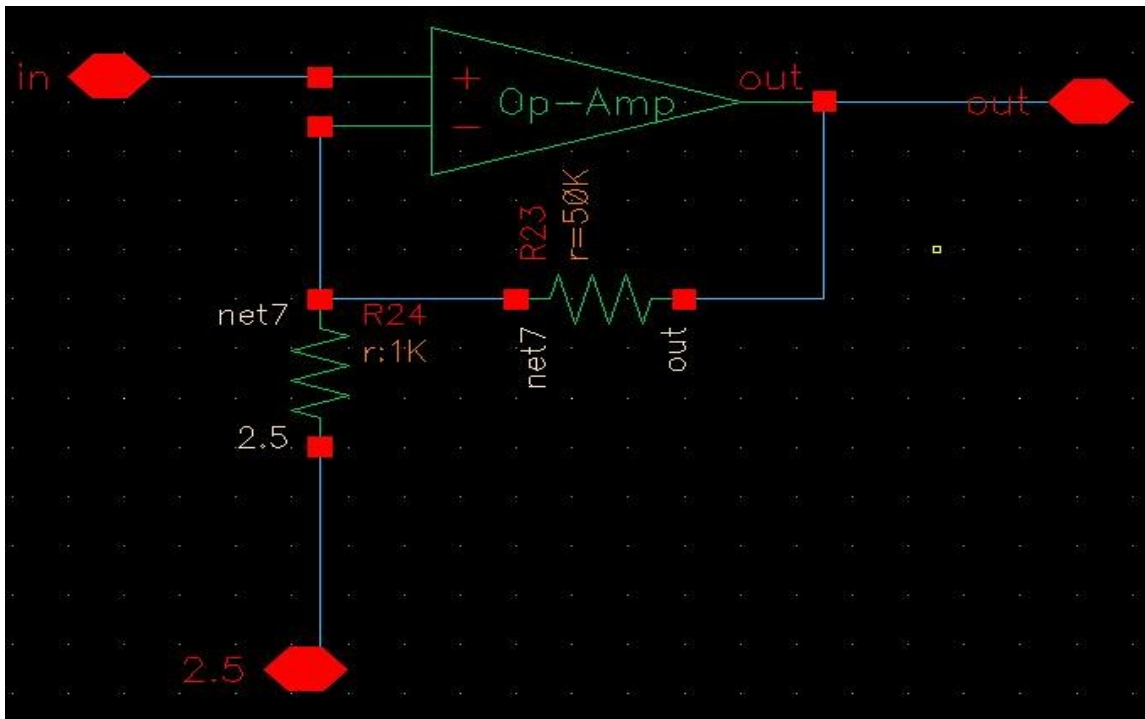
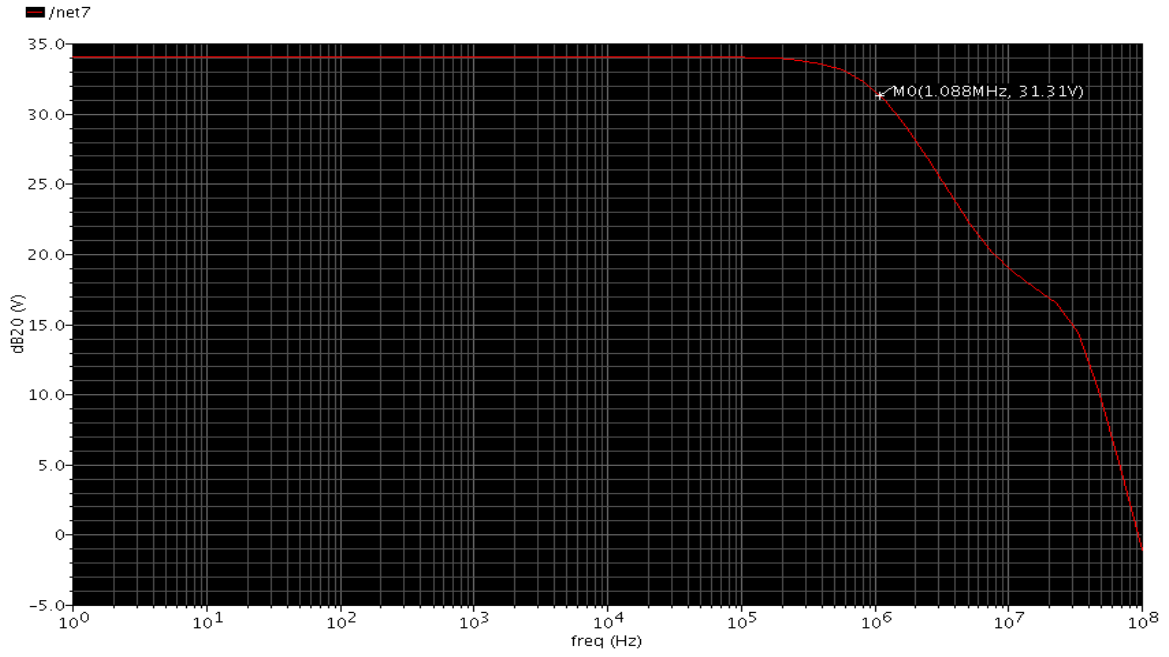


Figure 17: Amplifier Schematic



Graph 4: Frequency Response of Amplifier

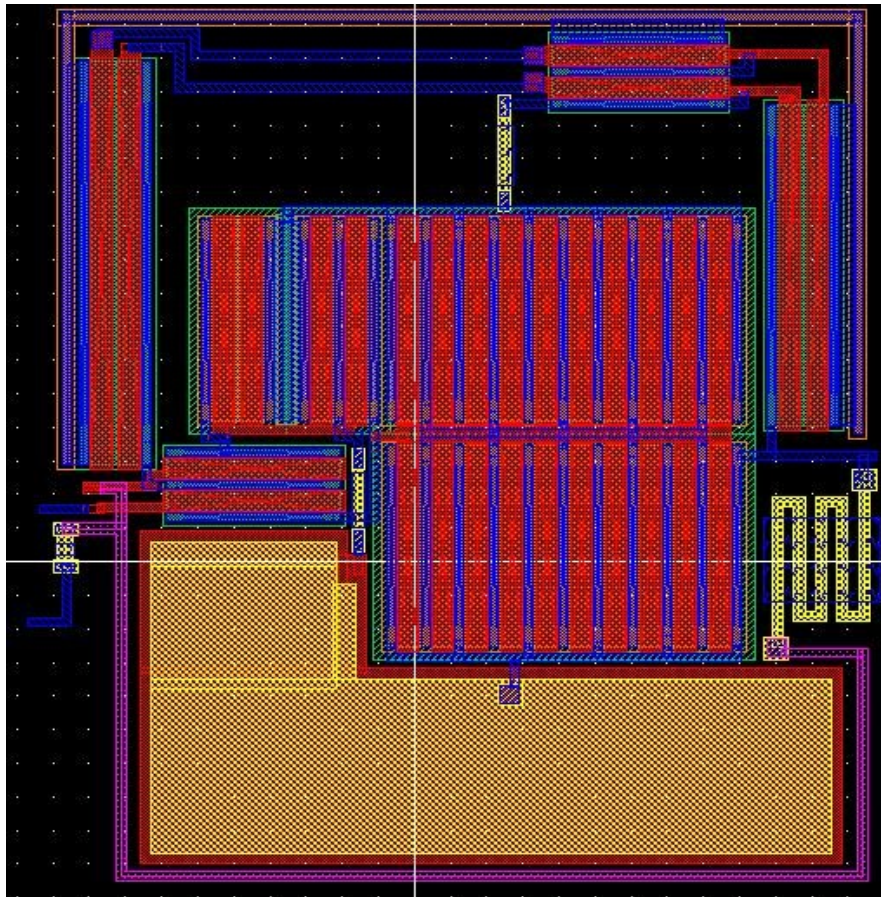


Figure 18: Amplifier Layout

G. Schmitt Trigger

The Schmitt Trigger is used to create a 0-5 Volt signal which will be taken into a PIC chip and be decoded. Unlike the original design, this design will use a six transistor design. To determine the trigger values, two equations were used to set the transistor sizes. The lower three transistors (see figure 19) sets upper threshold voltage; the upper three sets the lower threshold voltage. The following equations set these values, equation 1 sets the transistor sizes for the lower transistors, and equation 2 sets the upper transistors.

$$W1/W3 = [(V_{dd} - V_{sph}) / (V_{sph} - V_{thn})]^2 \quad (1)$$

$$W5/W6 = [(V_{spl}) / (V_{dd} - V_{spl} - V_{thp})]^2 \quad (2)$$

For this, $V_{dd} = 5 \text{ V}$, $V_{sph} = 2.55 \text{ V}$, $V_{spl} = 2.45 \text{ V}$, $V_{thn} = V_{thp} = .25 \text{ V}$. With that, the width ratios are found to be 1.96 in both equations. It should be noted that the transistor values are based from the book¹, in the schematic, transistors 1-3 are the nmos, 4-6 are the pmos, with 3 and 6 representing the ones to the right, 1 and 5 are at the extreme top and bottom, and 2 and 4 are in the middle. For transistors 2 and 4, those widths must be set at least larger than the smallest device, but not too large. In this case, they are in between. Figure 19 shows the schematic, Graph 5 shows the hysteresis plot of the trigger, and Figure 20 shows the layout.

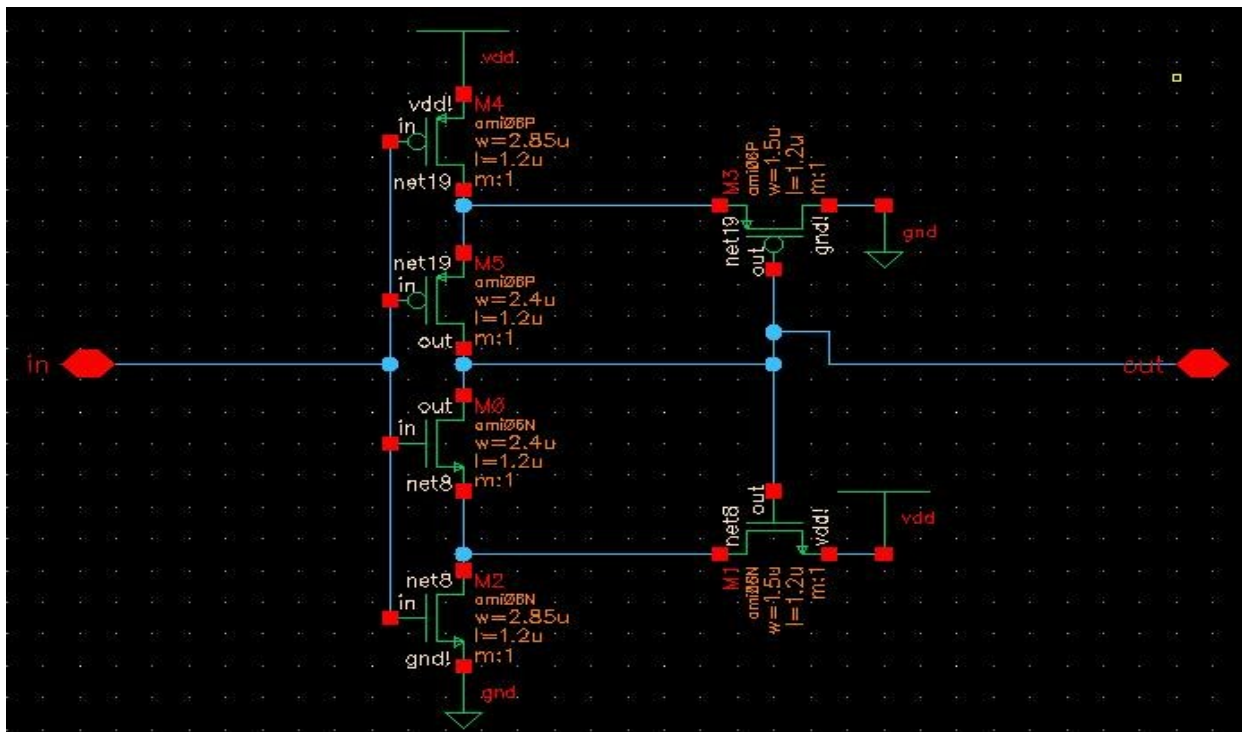
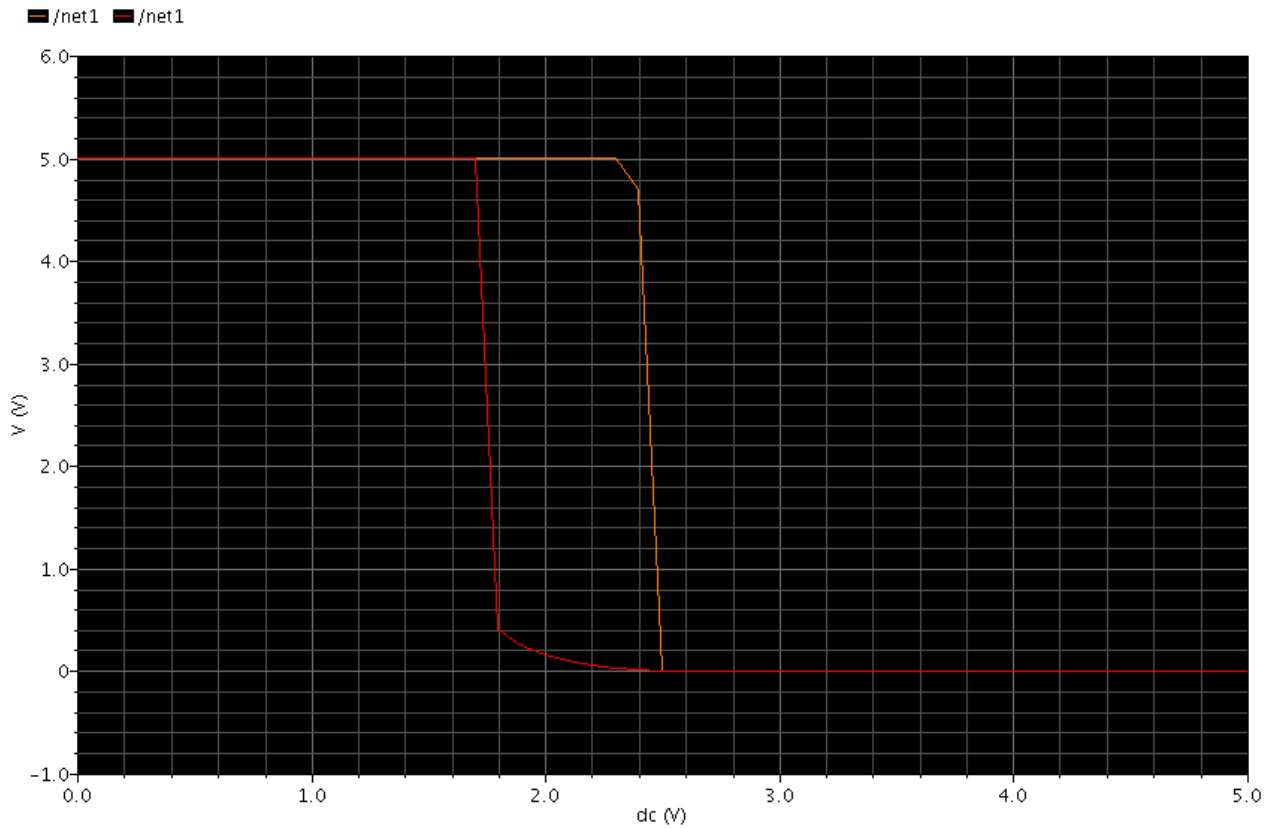


Figure 19: Schmitt Trigger Schematic



Graph 5: Hysteresis Plot of Trigger

In the graph above, the Orange plot is when the DC Voltage increases from 0 to 5 Volts, while the Red plot is when the DC Voltage decreases from 5 to 0 Volts.

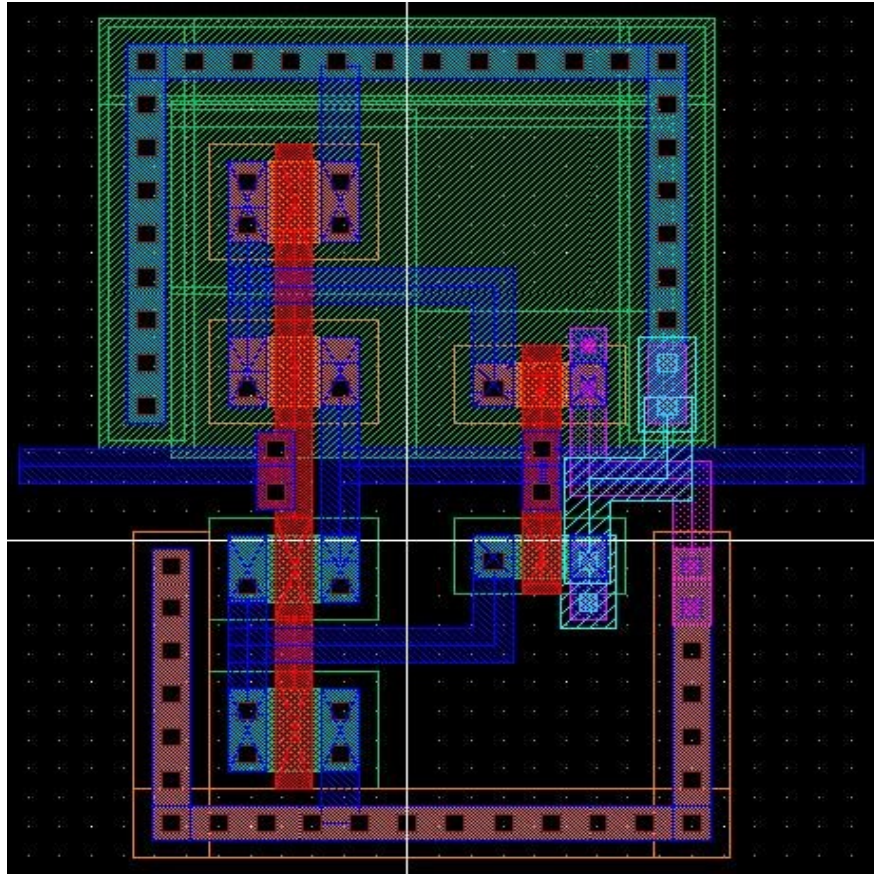


Figure 20: Schmitt Trigger Layout

H. Top-Level Design

Combining it all together gives a circuit block schematic like the one shown in Figure 21. The chip in its entirety, has two identical circuits like the one shown below.

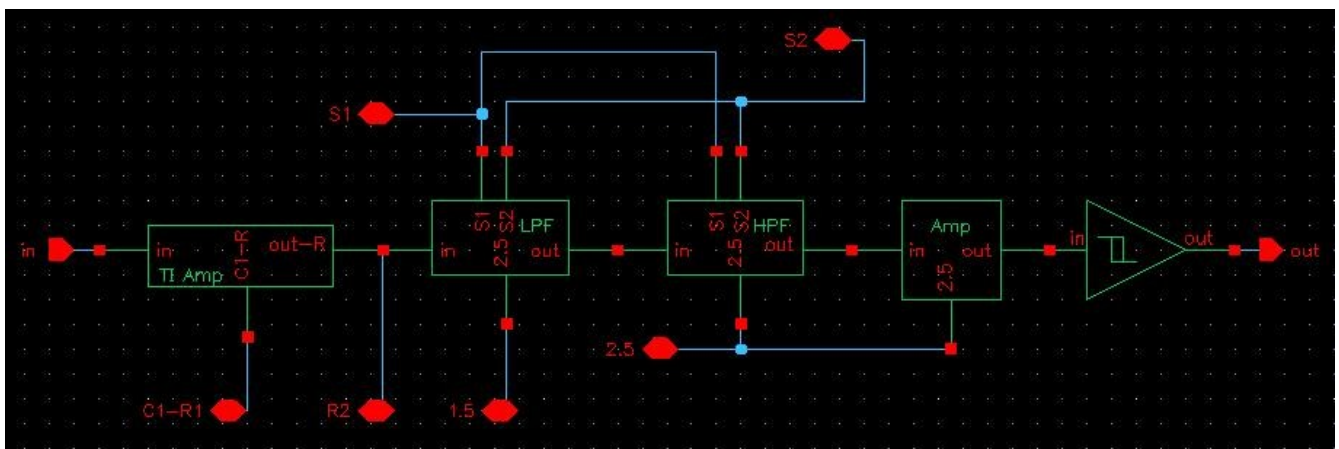


Figure 21: Top-Level Schematic

When taking this circuit into a layout, the overall size had to take into consideration of the ESD ring size. The overall layout of one circuit can be seen in its entirety in Figure 22.

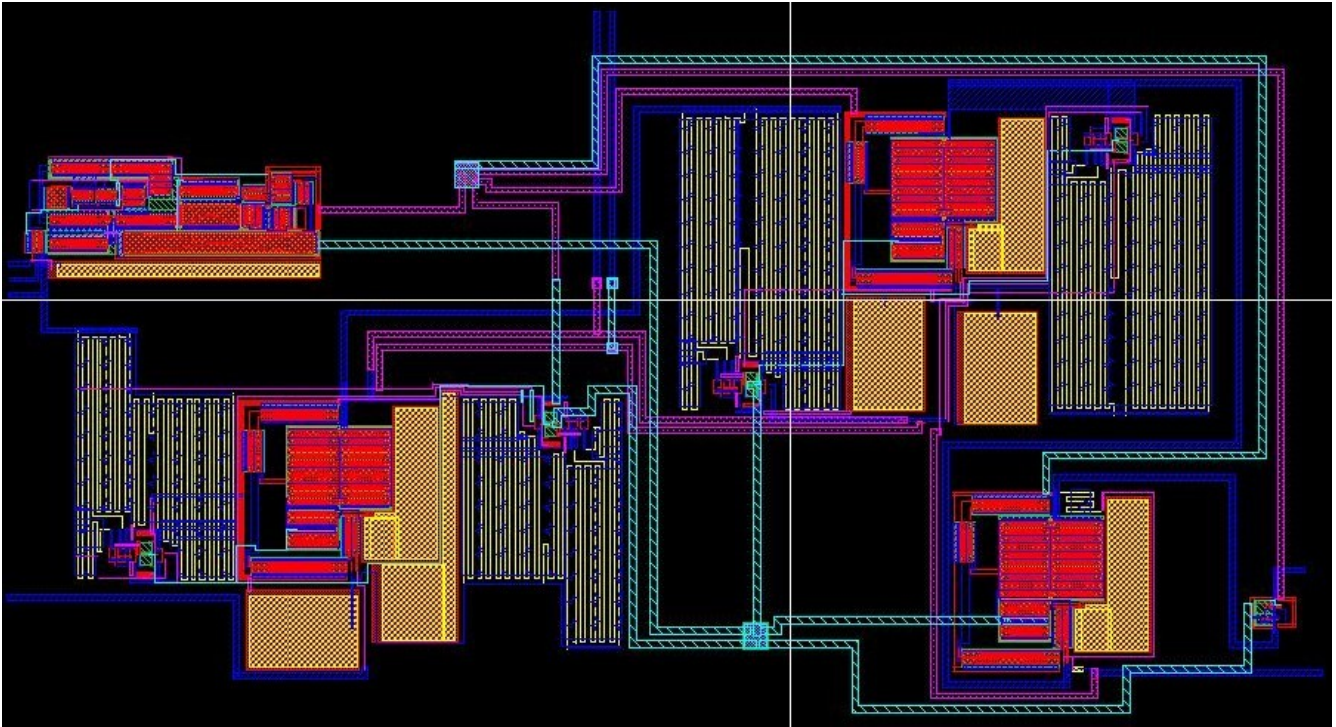


Figure 22: Complete Layout

On the ESD ring, all of the pins used in both circuits, with the exception of the outputs used a standard ESD pad (no additional buffer also known as “padaref”). The outputs had a pad with an added digital buffer. The issue with this pad was that it lacked a schematic, so a schematic was made based from the extracted results of the layout. Figure 23 (next page) shows the new schematic for the Digital Buffer ESD pad.

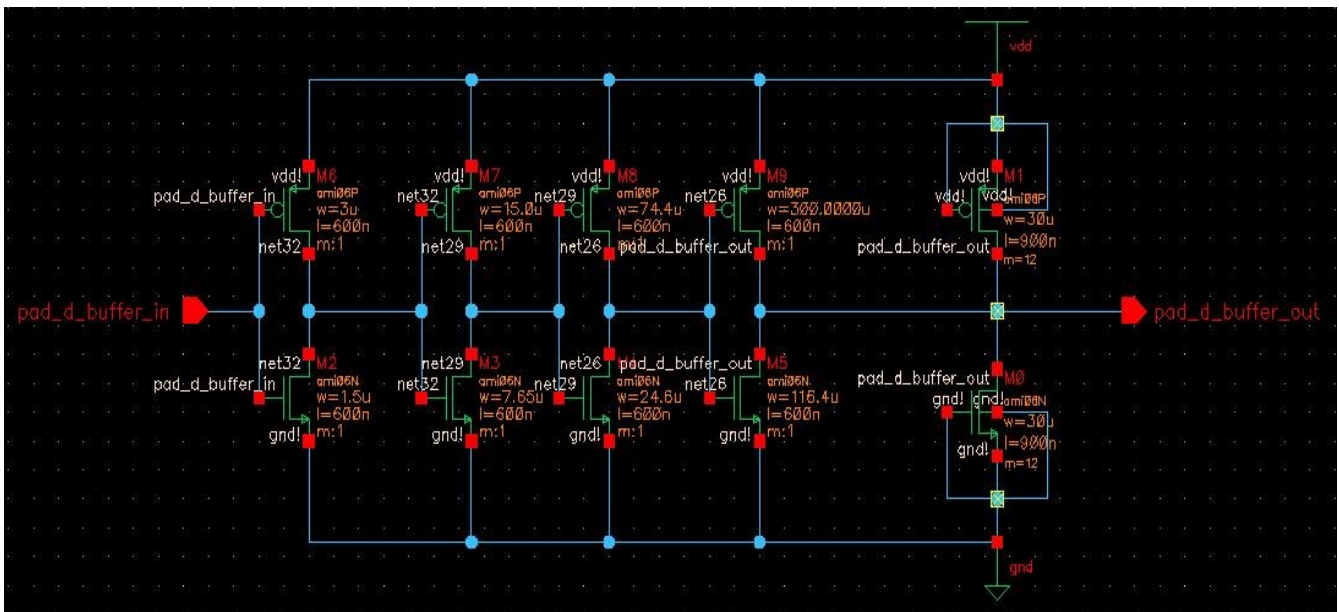


Figure 23: Digital Buffer Pad Schematic

In Figure 24 on the next page, shows the entire die that will be manufactured, all used pins with the exceptions of the output use the standard ESD pad (padaref). The remaining pads are not connected, but exist to continue the power and ground rings. Of the 40 pins available, 18 are used. When the layout was streamed-out, the results came back for fill rules with 14.4 out of 15% of poly, 55.1 out of 30% of Metall1, 54.5 out of 30% of metal2. Despite the .6% difference of poly, the design was accepted by MOSIS.

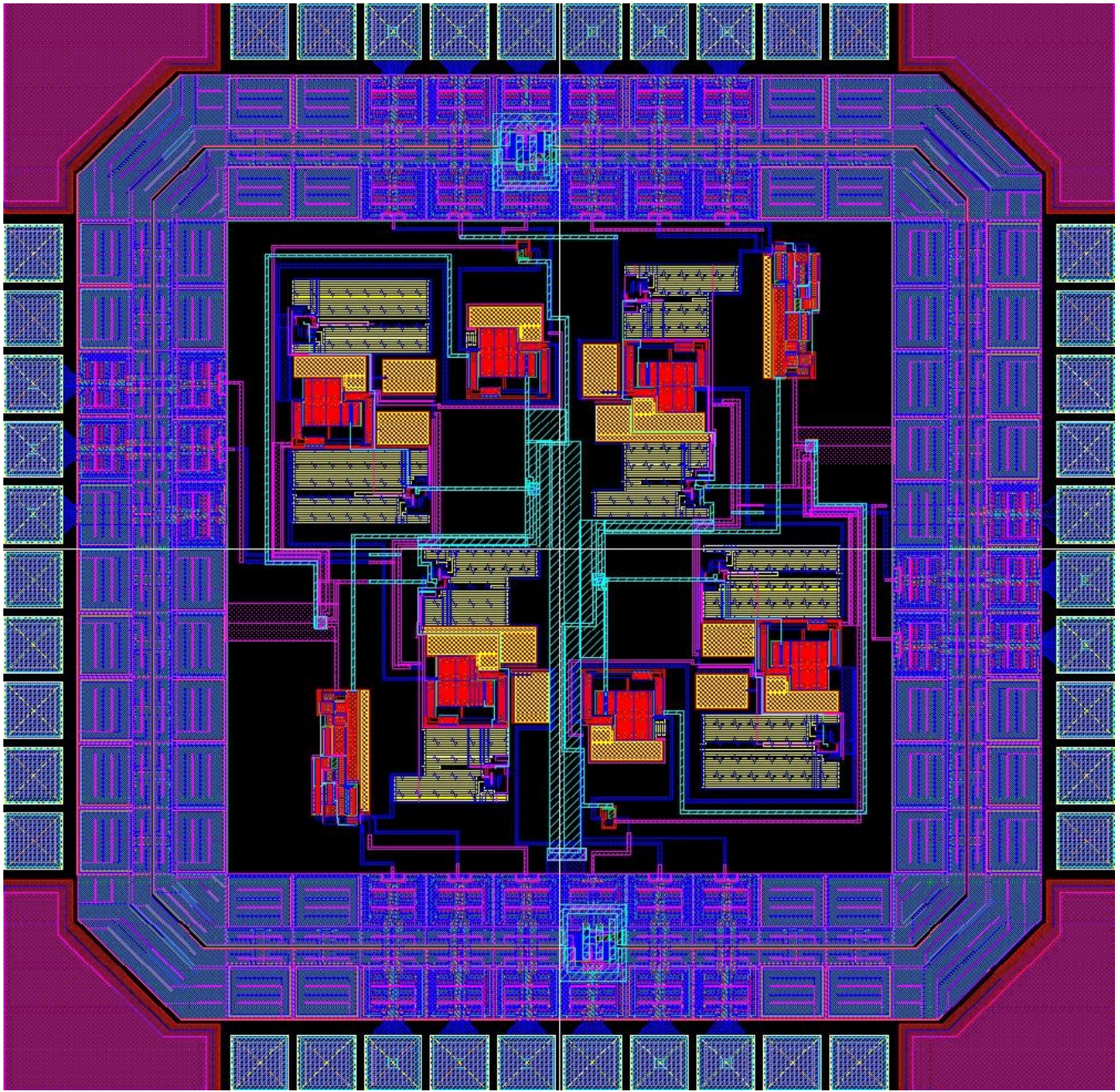
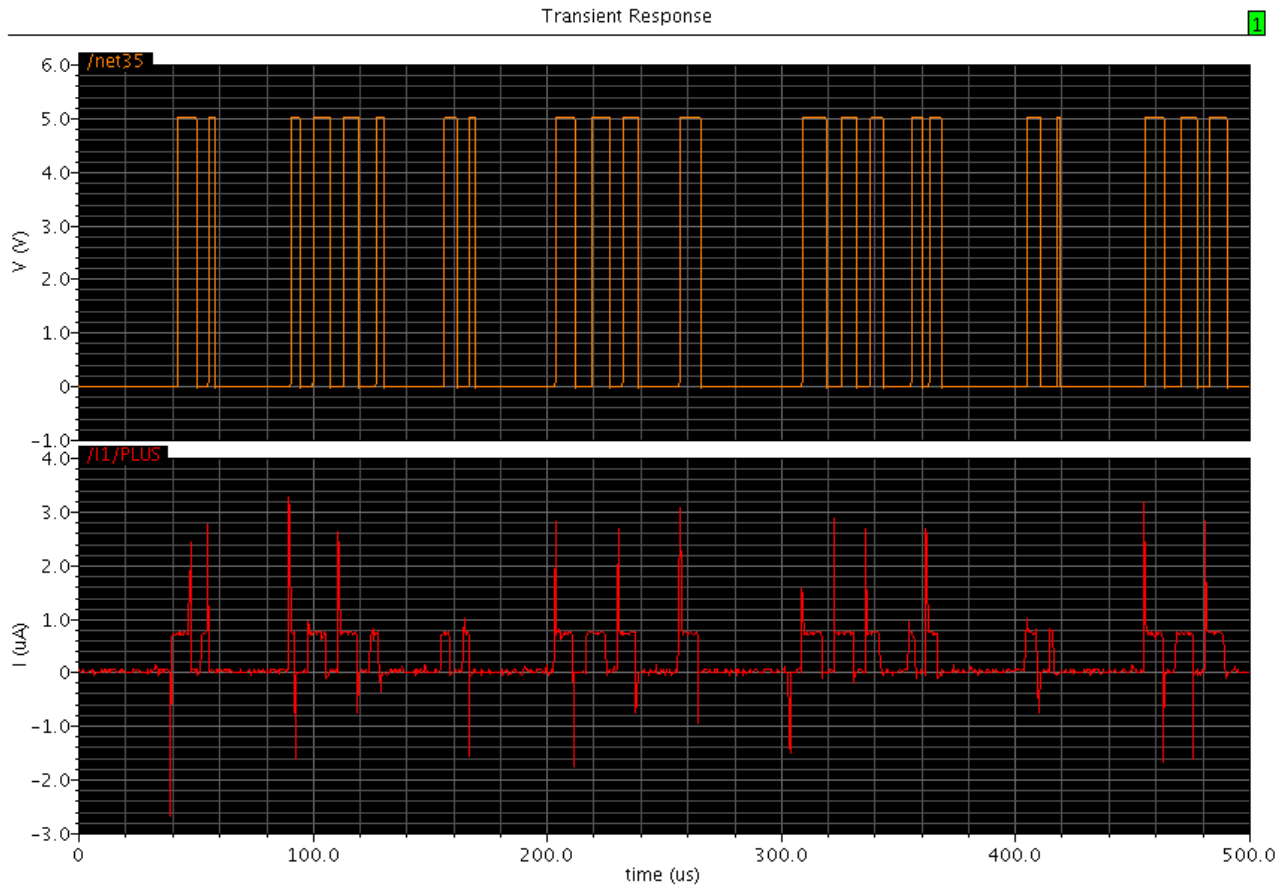


Figure 24: Complete Top-Level Layout

Upon passing Design Rules Check (DRC) and Layout vs Schematic (LVS) tests, an analog extracted of the layout with parasitic capacitors was used in the simulation by use of a config file. Using the analog extracted of the layout, and adding the impedance of the bonding wires, a simulation was taken, and the results are shown below in Graph 6. The figure has two simulations, the bottom shows the original current that was received, the upper shows the output signal from the chip. As can be seen the output shows nearly all of the important pulses. There is a small propagation delay 1-2 microseconds.



Graph 6: Chip Level Simulation (upper: Actual results; lower: Input current signal)

The schematic used is the one shown on the next page in Figure 25. This may appear to be confusing, but a simplified schematic is shown in Figure 26.

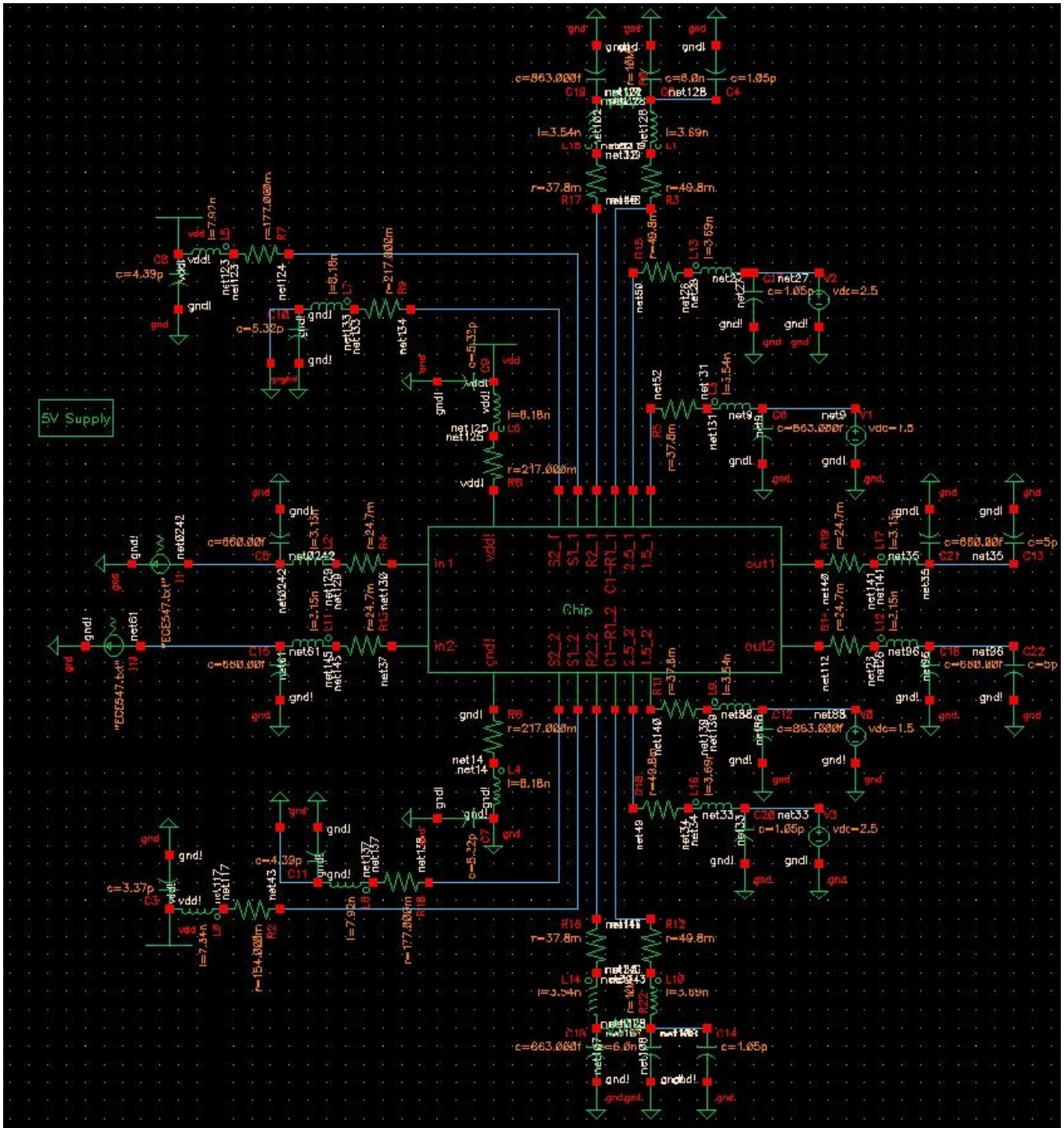


Figure 25: Chip Schematic with External Components

III. TESTING PROCEDURES

A. *Connecting the New Chip Design*

The following shows what pins are to be connected (x represents both 1 and 2), and how to connect them.

- 1.5_x: A voltage divider with a resistors ($R2/(R1+R2)$) is equal to .3, or set a source to 1.5 Volts
- 2.5_x: A voltage divider with equal resistor sizes or set a source to 2.5 Volts
- C1-R1_x & R2_x: Attach the 10M Ω resistors and the 6 nF capacitors as seen in Figure 33
- R2_x & out_x: Attach oscilloscope probes
- out_x: Attach a 5 pF capacitor (to represent a load)
- in_x: There are two options:
 - A. Attach a BPV10 PIN Photo diodes from Vishay in the orientation shown in Figure 33
 - B. Attach a pulse modulated signal at an amplitude of .5 μ A. The pulses should imitate the signal shown in Graph 6: lower (page 30) Which the pulses operate at 76.8 KHz
- S1_x: Set High to 5 Volts by use of the jumpers (for frequency of 76.8 KHz)
- S2_x: Set Low to 0 Volts by use of the jumpers (for frequency of 76.8 KHz)

B. *Input Signal*

B.1. *Option A*

Option A gives the most accurate signal, however operates at one carrier frequency only. To test if the chip is receiving the the signal, take the receiver board and place it at point-blank-range to the transmitter board (read below). Then move the board back until the signal cannot be seen, at this point, it would be maximum range.

The transmitter board has already been made, and has been supplied to Dr. Kotecki. This board will transmit an automated signal with a carrier frequency 76.8 KHz. The original receiver board (one with 8 red LEDs) is also available as a reference. Each board has three wires, which are used for power. The Red wire is for a +10 Volt supply, the Green wire is the -10 Volt supply, and the Black wire is for ground. Once power is supplied, the transmitter will send the message automatically. For testing the IR Receiver chip, the receiver board is not necessary but is only used as a reference and a test for the transmitter, to check if the transmitter is working. To determine if the transmitter is working, connect the receiver, and power it on, and place the board approximately 10 feet away (as the ECE 403 specifications require). On the board, the 8 LEDs will turn on upon powering. To determine if it is

receiving, the LEDs will dim, as they will be turning on and off at real time speeds. This can be easier seen when the room lights are turned off or lowered.

B.2. Option B

Option B must use a current pulse source with the following settings. When switching to different carrier frequencies, change the S1_x and S2_x pins to what is shown in Tables 1 (page 9) and 2 (page 11). Start the current amplitude must start at .1 μ A and increase upto 1mA, or until the circuit does not give an output like the one shown in Graph 6 (upper).

C. Transimpedance Amplifier Test

The scope probe located at the R2_x pins show the output of the transimpedance amplifier. If it shows a signal response similar to the result shown in Graph 3 (lower), then it is known that the transimpedance amplifier is working correctly.

D. Overall Chip Test

With the chip receiving a current signal on the input, the output is already showing a result.

Test by sweeping:

- A. The distance (if using Option A), or
- B. The current amplitude range (if using Option B) from .1 μ A up to 1 mA.

The output should result into a 0-5 pulse signal operating at the same (or near to same) frequency as the carrier frequency.

The following are cases of failure:

1. Output signal does not go to 0-5 Volts. This acceptable as long as the maximum amplitude is greater than 2 Volts. The reason to failure is do to being out of range (option A), or has too little current (option B)
2. (In Option A only) The output signal has noise embedded in the signal. The reason of failure is due to the gain is too high that for a certain point in the distance. The input signal to the Schmitt Trigger has noise that did not filter correctly, thus exists, and is also amplified. The noise is acceptable until the noise either affects the primary pulses or the noise is greater than 2 Volts.

IV. CONCLUSION

The design of the IR Receiver Demodulator is completed through the stages of design, simulation, and layout. The specifications of the project that were stated in the Introduction were accomplished, and testing of a real signal has confirmed the circuit will operate correctly at the carrier frequencies of 38.4, 76.8, 153.6 and 307.2 Khz. The layout passed both DRC and LVS at the top level, and sent for fabrication and will be ready for testing in the Fall of 2008.

A. Possible Improvements for Future Work

One of three improvements that can be done is converting the bandpass filter to a Butterworth Filter with a high order. Also moving the cutoff frequencies further off, so the attenuation caused at the carrier frequencies become non-existent. The advantage to these improvements would have a more ideal bandpass filter while having a single Op-Amp being used.

The second improvement would be to add a transmitter component instead of having a dual receiver design. This would allow two-way communications and some of the same improvements that were made in this project. This would be more beneficial if the software package would support BJT devices.

The last improvement would be to optimize the performance of the Op-Amp, with higher bandwidth, gain, and phase margin, while maintaining high slew rate

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